ATCA-7365-CE

Installation and Use

P/N: 6806800L73M

September 2015

ARTESYN™

EMBEDDED TECHNOLOGIES

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About this Manual

Overview of Contents

This Reference Guide is intended for users qualified in electronics or electrical engineering. Users must have a working understanding of Peripheral Component Interconnect (PCI), AdvancedTCA®, and telecommunications.

The manual contains the following chapters and appendices:

- *About this Manual* on page 19 lists all conventions and abbreviations used in this manual and outlines the revision history.
- *Safety Notes* on page 27 lists safety notes applicable to the blade.
- *Sicherheitshinweise* on page 31 provides the German translation of the safety notes.
- *Introduction* on page 37 describes the main features, Standard Compliances, Mechanical data, and ordering information of the blade.
- *Hardware Preparation and Installation* on page 45 outlines the installation requirements, hardware accessories, switch settings, installation and removal procedures.
- *Controls, Indicators, and Connectors* on page 65 describes external interfaces of the blade. This includes connectors and LEDs.
- *BIOS* on page 87 describes the features and setup of BIOS.
- *Functional Description* on page 143 describes the functional blocks of the blade in detail. This includes a block diagram, description of the main components used and so on.
- *Maps and Registers* on page 155 provides information on the blade's maps and registers.
- *Serial Over LAN* on page 215 provides information on how to establish a serial-over LAN session on your blade.
- *Supported IPMI Commands* on page 221 lists all supported IPMI commands.
- *FRU Information and Sensor Data Records* on page 261 provides information on the blade's FRU information and sensor data.
- *Firmware Upgrade* on page 277 provides information on how to upgrade the firmware components.
- *Replacing the Battery* on page 283 provides the battery exchange procedures.
- *Related Documentation* on page 287 provides links to further blade related documentation.

Abbreviations

This document uses the following abbreviations:

Abbreviation	Definition
ANSI	American National Standards Institute
API	Application Programming Interface
APIC	Advanced Programmable Interrupt Controller
ATA	Advanced Technology Attachment
ATCA	Advanced Telecommunications Computing Architecture
BIOS	Basic Input/Output System
CAS	Column Address Strobe
CMOS	Complementary Metal Oxide Semiconductor
DDR	Double Data Rate
DIMM	Dual Inline Memory Module
DMA	Direct Memory Access
DPLL	Digital Phase Locked Loop
DRAM	Dynamic Random Access Memory
ECC	Error-Correction Code
EMC	Electromagnetic Compatibility
EMV	Elektromagnetische Vertraeglichkeit
EN	European Norm
ESCD	Extended System Configuration Data
ESD	Electrostatic Sensitive Device
FAE	Field Application Engineers
FC	Fibre Channel
FCC	Federal Communications Commission
FIFO	First In First Out
FPGA	Field-Programmable Gate Array
FRU	Field Replaceable Unit

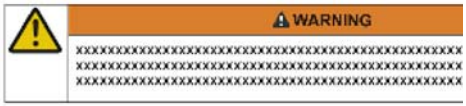
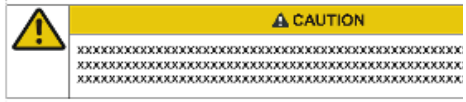
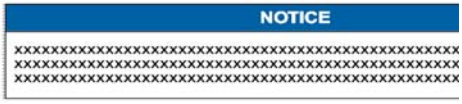
Abbreviation	Definition
GND	Ground
GmbH	Gesellschaft mit beschraenkter Haftung
HDD	Hard Disk Drive
I2C	Inter-Integrated Circuit
IDE	Integrated Device Electronics
IEC	International Electric Code
IEEE	Institute of Electrical and Electronics Engineers
IPMB	Intelligent Platform Management Bus
IPMC	Intelligent Platform Management Controller
IPMI	Intelligent Platform Management Interface
ISA	Industry Standard Architecture
ISO	International Organization for Standardization
LCCB	Line Card Clock Building Block
LFM	Linear Feet per Minute
LPC	Low Pin Count
MAC	Media Access Control
MTD	Memory Technology Device
MVCGE	MontaVista Carrier Grade Edition
NEBS	Network Equipment Building System
NMI	Non-Maskable Interrupt
NVRAM	Non-volatile Random Access Memory
OEM	Original Equipment Manufacturer
OOS	Out-Of-Service
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PEM	Power Entry Module
PICMG	PCI Industrial Computer Manufacturers Group
PMC	PCI Mezzanine Card

Abbreviation	Definition
POST	Power-On Self-Test
PROM	Programmable Read-Only Memory
PTMC	PCI Telecom Mezzanine Card
PXE	Preboot Execution Environment
RHEL	Red Hat Enterprise Linux
RMCP	Remote Management Control Protocol
RTC	Real Time Clock
RTM	Rear Transition Module
RoHS	Restriction of the use of Certain Hazardous Substances
SAS	Serial Attached SCSI
SATA	Serial ATA
SCSI	Small Computer System Interface
SDR	Sensor Data Record
SDRAM	Synchronous Dynamic Random Access Memory
SELV	Safety Extra Low Voltages
SMI	Serial Management Interface
SOL	Serial-over-LAN
SPD	Serial Presence Detect
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SROM	Serial Read-Only Memory
UL	Underwriters Laboratory Inc.
VGA	Video Graphics Array
VLAN	Virtual Local Area Network

Conventions

The following table describes the conventions used throughout this manual.

Notation	Description
0x00000000	Typical notation for hexadecimal numbers (digits are 0 through F), for example used for addresses and offsets
0b0000	Same for binary numbers (digits are 0 and 1)
bold	Used to emphasize a word
`Screen`	Used for on-screen output and code related elements or commands in body text
`Courier + Bold`	Used to characterize user input and to separate it from system output
Reference	Used for references and for table and figure descriptions
File > Exit	Notation for selecting a submenu
<text>	Notation for variables and keys
[text]	Notation for software buttons to click on the screen and parameter description
...	Repeated item for example node 1, node 2, ..., node 12
. . .	Omission of information from example/command that is not necessary at the time being
..	Ranges, for example: 0..4 means one of the integers 0,1,2,3, and 4 (used in registers)
|	Logical OR

Notation	Description
	Indicates a hazardous situation which, if not avoided, could result in death or serious injury
	Indicates a hazardous situation which, if not avoided, may result in minor or moderate injury
	Indicates a property damage message
	No danger encountered. Pay attention to important information

Summary of Changes

Part Number	Publication Date	Description
6806800L73M	September 2015	Updated the sections *Standard Compliances* on page 38, *Installation* on page 28, and *Installation* on page 32.
6806800L73L	June 2015	Updated the section *Environmental Requirements* on page 46.
6806800L73K	January 2015	Updated the Figure "Location of Critical Temperature Spots" on page 48 and PWR Entry Status information in Table "Sensor Data Records" on page 270.
6806800L73J	May 2014	Re-branded to Artesyn.
6806800L73H	February 2014	Updated Table 9-8 on page 270 and Table 3-1 on page 69. Updated Table 8-33 on page 250 and Table 8-34 on page 251.
6806800L73G	February 2013	Updated Table 2-4 on page 53.
6806800L73F	January 2013	Updated *Standard Compliances* on page 38.
6806800L73E	April 2012	Added a note in *DIMM Memory Modules* on page 55. Updated Table 6-7, *Using ipmitool* on page 217, and Table 8-16.
6806800L73D	March 2012	Added a Notice in *Installation* on page 28 and *Installation* on page 32. Updated Table 2-4. Updated *Standard Compliances* on page 38, *EMC* on page 27 and *EMV* on page 32.
6806800L73C	September 2011	Updated Chapter 4, *BIOS, on page 87*. Added Chapter 4, *iSCSI Setup for Base and Fabric Ethernet, on page 94*. Updated Table "CPU Configuration" on page 100. Updated Table "BIOS Supported IPMI Events" on page 123. Updated Table "Result Second DWORD supported POST Errors" on page 128. Updated Table "Sensor Data Records" on page 270. Edited Figure "Location of AdvancedTCA Connectors" on page 80.
6806800L73B	August 2011	Updated *Serial Interface Connector* on page 72
6806800L73A	December 2010	GA version

Safety Notes

This section provides warnings that precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed during all phases of operation, service, and repair of this equipment. You should also employ all other safety precautions necessary for the operation of the equipment in your operating environment. Failure to comply with these precautions or with specific warnings elsewhere in this manual could result in personal injury or damage to the equipment.

Artesyn Embedded Technologies intends to provide all necessary information to install and handle the product in this manual. Because of the complexity of this product and its various uses, we do not guarantee that the given information is complete. If you need additional information, ask your Artesyn representative.

The product has been designed to meet the standard industrial safety requirements. It must not be used except in its specific area of office telecommunication industry and industrial control.

Only personnel trained by Artesyn or persons qualified in electronics or electrical engineering are authorized to install, remove or maintain the product.

The information given in this manual is meant to complete the knowledge of a specialist and must not be used as replacement for qualified personnel.

Keep away from live circuits inside the equipment. Operating personnel must not remove equipment covers. Only factory authorized service personnel or other qualified service personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment.

Do not install substitute parts or perform any unauthorized modification of the equipment or the warranty may be voided. Contact your local Artesyn representative for service and repair to make sure that all safety features are maintained.

EMC

The blade has been tested in a standard Artesyn system and found to comply with the limits for a Class A digital device in this system, pursuant to part 15 of the FCC Rules, EN 55022 Class A respectively. These limits are designed to provide reasonable protection against harmful interference when the system is operated in a commercial environment.

This is a Class A product based on the standard of the Voluntary Control Council for Interference by Information Technology Interference (VCCI). If this equipment is used in a domestic environment, radio disturbance may arise. When such trouble occurs, the user may be required to take corrective actions.

To ensure EMC protection use only shielded cables when connecting peripherals to assure that appropriate radio frequency emissions compliance is maintained. Installed blades must have the faceplates installed and all vacant slots in the shelf must be covered.

The blade generates and uses radio frequency energy and, if not installed properly and used in accordance with this guide, may cause harmful interference to radio communications. Operating the system in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his own expense.

Installation

Damage of Circuits
Electrostatic discharge and incorrect blade installation and removal can damage circuits or shorten their life.
Before touching the blade or electronic components, make sure that you are working in an ESD-safe environment.

Data Loss
Removing the blade with the blue LED still blinking causes data loss.
Wait until the blue LED is permanently illuminated, before removing the blade.

Damage of Blade and Additional Devices and Modules
Incorrect installation of additional devices or modules may damage the blade or the additional devices or modules.
Before installing or removing an additional device or module, read the respective documentation

System Damage
WARNING: The intra-building port (s) of the equipment or subassembly is suitable for connection to intra-building or unexposed wiring or cabling only. The intra-building port (s) of the equipment or subassembly MUST NOT be metallically connected to interfaces that connect to the outside plant (OSP) or its wiring. These interfaces are designed for use as intra-building interfaces only (Type 2 or Type 4 ports as described in GR-1089) and require isolation from the exposed OSP cabling. The addition of primary protectors is not sufficient protection in order to connect these interfaces metallically to OSP wiring.
The intra-building port (s) of the equipment or subassembly must use shielded intra-building cabling/wiring that is grounded at both ends.

Operation

Ensure that the display devices that are permanently connected to the VGA interface provide a fire enclosure according to the IEC/EN/UL/CSA 60950-1 requirements.
All other devices that are connected only for service purposes to the VGA interface needs supervision during operation and must be disconnected after maintenance.

Blade Damage
Blade surface
High humidity and condensation on the blade surface causes short circuits.
Do not operate the blade outside the specified environmental limits. Make sure the blade is completely dry and there is no moisture on any surface before applying power.

Blade Overheating and Blade Damage
Operating the blade without forced air cooling may lead to blade overheating and thus blade damage.
When operating the blade, make sure that forced air cooling is available in the shelf.

When operating the blade in areas of electromagnetic radiation ensure that the blade is bolted on the system and the system is shielded by enclosure.

Injuries or Short Circuits
Blade or power supply

In case the ORing diodes of the blade fail, the blade may trigger a short circuit between input line A and input line B so that line A remains powered even if it is disconnected from the power supply circuit (and vice versa).
To avoid damage or injuries, always check that there is no more voltage on the line that has been disconnected before continuing your work.

Switch Settings

Blade Malfunction
Switches marked as 'reserved' might carry production-related functions and can cause the blade to malfunction if their setting is changed.
Therefore, do not change settings of switches marked as 'reserved'. The setting of switches which are not marked as 'reserved' has to be checked and changed before blade installation.

Blade Damage
Setting/resetting the switches during operation can cause blade damage.
Therefore, check and change switch settings before you install the blade.

Battery

Blade Damage
Wrong battery installation may result in hazardous explosion and blade damage.
Therefore, always use the same type of Lithium battery as is installed and make sure the battery is installed as described in this manual.

Environment

Always dispose of used blades, system components and RTMs according to your country's legislation and manufacturer's instructions.

Sicherheitshinweise

Dieses Kapitel enthält Hinweise, die potentiell gefährlichen Prozeduren innerhalb dieses Handbuchs vorrangestellt sind. Beachten Sie unbedingt in allen Phasen des Betriebs, der Wartung und der Reparatur des Systems die Anweisungen, die diesen Hinweisen enthalten sind. Sie sollten außerdem alle anderen Vorsichtsmaßnahmen treffen, die für den Betrieb des Produktes innerhalb Ihrer Betriebsumgebung notwendig sind. Wenn Sie diese Vorsichtsmaßnahmen oder Sicherheitshinweise, die an anderer Stelle diese Handbuchs enthalten sind, nicht beachten, kann das Verletzungen oder Schäden am Produkt zur Folge haben.

Artesyn Embedded Technologies ist darauf bedacht, alle notwendigen Informationen zum Einbau und zum Umgang mit dem Produkt in diesem Handbuch bereit zu stellen. Da es sich jedoch um ein komplexes Produkt mit vielfältigen Einsatzmöglichkeiten handelt, können wir die Vollständigkeit der im Handbuch enthaltenen Informationen nicht garantieren. Falls Sie weitere Informationen benötigen sollten, wenden Sie sich bitte an die für Sie zuständige Geschäftsstelle von Artesyn.

Das System erfüllt die für die Industrie geforderten Sicherheitsvorschriften und darf ausschließlich für Anwendungen in der Telekommunikationsindustrie und im Zusammenhang mit Industriesteuerungen verwendet werden.

Einbau, Wartung und Betrieb dürfen nur von durch Artesyn ausgebildetem oder im Bereich Elektronik oder Elektrotechnik qualifiziertem Personal durchgeführt werden. Die in diesem Handbuch enthaltenen Informationen dienen ausschließlich dazu, das Wissen von Fachpersonal zu ergänzen, können dieses jedoch nicht ersetzen.

Halten Sie sich von stromführenden Leitungen innerhalb des Produktes fern. Entfernen Sie auf keinen Fall Abdeckungen am Produkt. Nur werksseitig zugelassenes Wartungspersonal oder anderweitig qualifiziertes Wartungspersonal darf Abdeckungen entfernen, um Komponenten zu ersetzen oder andere Anpassungen vorzunehmen.

Installieren Sie keine Ersatzteile oder führen Sie keine unerlaubten Veränderungen am Produkt durch, sonst verfällt die Garantie. Wenden Sie sich für Wartung oder Reparatur bitte an die für Sie zuständige Geschäftsstelle von Artesyn. So stellen Sie sicher, dass alle sicherheitsrelevanten Aspekte beachtet werden.

EMV

Das Blade wurde in einem Artesyn Standardsystem getestet. Es erfüllt die für digitale Geräte der Klasse A gültigen Grenzwerte in einem solchen System gemäß den FCC-Richtlinien Abschnitt 15 bzw. EN 55022 Klasse A. Diese Grenzwerte sollen einen angemessenen Schutz vor Störstrahlung beim Betrieb des Blades in Gewerbe- sowie Industriegebieten gewährleisten.

Das Blade arbeitet im Hochfrequenzbereich und erzeugt Störstrahlung. Bei unsachgemäßem Einbau und anderem als in diesem Handbuch beschriebenen Betrieb können Störungen im Hochfrequenzbereich auftreten.

Benutzen Sie zum Anschließen von Peripheriegeräten ausschließlich abgeschirmte Kabel. So stellen Sie sicher, dass ausreichend Schutz vor Störstrahlung vorhanden ist. Die Blades müssen mit der Frontblende installiert und alle freien Steckplätze müssen mit Blindblenden abgedeckt sein.

Warnung! Dies ist eine Einrichtung der Klasse A. Diese Einrichtung kann im Wohnbereich Funkstörungen verursachen. In diesem Fall kann vom Betreiber verlangt werden, angemessene Maßnahmen durchzuführen.

Installation

Beschädigung von Schaltkreisen
Elektrostatische Entladung und unsachgemäßer Ein- und Ausbau von Blades kann Schaltkreise beschädigen oder ihre Lebensdauer verkürzen.
Bevor Sie Blades oder elektronische Komponenten berühren, vergewissern Sie sich, daß Sie in einem ESD-geschützten Bereich arbeiten.

Datenverlust
Wenn Sie das Blade aus dem Shelf herausziehen, und die blaue LED blinkt noch, gehen Daten verloren.
Warten Sie bis die blaue LED durchgehend leuchtet, bevor Sie das Blade herausziehen.

Beschädigung des Blades und von Zusatzmodulen
Fehlerhafte Installation von Zusatzmodulen, kann zur Beschädigung des Blades und der Zusatzmodule führen.
Lesen Sie daher vor der Installation von Zusatzmodulen die zugehörige Dokumentation.

Beschädigung des Systems
Warnung: Die intra-Gebäude Port (s) des Geräts oder Baugruppe ist für den Anschluss an den inner Gebäude oder unbelichteten Verdrahtung oder Verkabelung nur. Die intra-Gebäude Port(s) des Geräts oder Baugruppe muss nicht metallisch mit Schnittstellen, die an der Außenanlage (OSP) oder dessen Verkabelung anschließen angeschlossen werden. Diese Schnittstellen sind für die Verwendung als intra Gebäude Schnittstellen nur entworfen, (Typ 2 oder Typ 4 Ports wie in GR-1089 beschrieben) und erfordern Isolierung von der freiliegenden OSP-Verkabelung. Die Zugabe von primären Schutz nicht ausreichenden Schutz, um diese Schnittstellen metallisch mit OSP Verdrahtung verbinden.
Die intra-Gebäude Port (s) des Gerätes oder einer Unterbaugruppe müssen abgeschirmte innerGebäudeVerkabelung / Verdrahtung, die an beiden Enden geerdet ist zu verwenden.

Betrieb

Stellen Sie sicher, daß Geräte, die dauerhaft mit der VGA Schnittstelle verbunden, sind über ein Brandschutzgehäuse verfügen, die die Anforderungen der IEC/EN/UL/CSA 60950-1 Norm erfüllen.
Alle anderen Geräte, die nur zeitweise für Wartungsarbeiten an die VGA Schnittstelle angeschlossen werden, müssen während dem Betrieb überwacht und nach der Beendigung der Wartungsarbeiten entfernt werden.

Beschädigung des Blades
Hohe Luftfeuchtigkeit und Kondensat auf der Oberfläche des Blades können zu Kurzschlüssen führen.
Betreiben Sie das Blade nur innerhalb der angegebenen Grenzwerte für die relative Luftfeuchtigkeit und Temperatur. Stellen Sie vor dem Einschalten des Stroms sicher, dass sich auf dem Blade kein Kondensat befindet.

Überhitzung und Beschädigung des Blades
Betreiben Sie das Blade ohne Zwangsbelüftung, kann das Blade überhitzt und schließlich beschädigt werden.
Bevor Sie das Blade betreiben, müssen Sie sicher stellen, dass das Shelf über eine Zwangskühlung verfügt.

Wenn Sie das Blade in Gebieten mit starker elektromagnetischer Strahlung betreiben, stellen Sie sicher, dass das Blade mit dem System verschraubt ist und das System durch ein Gehäuse abgeschirmt wird.

Verletzungen oder Kurzschlüsse
Blade oder Stromversorgung
Falls die ORing Dioden des Blades durchbrennen, kann das Blade einen Kurzschluss zwischen den Eingangsleitungen A und B verursachen. In diesem Fall ist Leitung A immer noch unter Spannung, auch wenn sie vom Versorgungskreislauf getrennt ist (und umgekehrt).
Prüfen Sie deshalb immer, ob die Leitung spannungsfrei ist, bevor Sie Ihre Arbeit fortsetzen, um Schäden oder Verletzungen zu vermeiden.

Schaltereinstellungen

Fehlfunktion des Blades
Schalter, die mit 'Reserved' gekennzeichnet sind, können mit produktionsrelevanten Funktionen belegt sein. Das Ändern dieser Schalter kann im normalen Betrieb Störungen auslösen.
Verstellen Sie nur solche Schalter, die nicht mit 'Reserved' gekennzeichnet sind. Prüfen und ändern Sie die Einstellungen der nicht mit 'Reserved' gekennzeichneten Schalter, bevor Sie das Blade installieren.

Beschädigung der Blade
Das Verstellen von Schaltern während des laufenden Betriebes kann zur Beschädigung des Blades führen.
Prüfen und ändern Sie die Schaltereinstellungen, bevor Sie das Blade installieren.

Batterie

Beschädigung des Blades
Ein unsachgemäßer Einbau der Batterie kann gefährliche Explosionen und Beschädigungen des Blades zur Folge haben.
Verwenden Sie deshalb nur den Batterietyp, der auch bereits eingesetzt wurde und befolgen Sie die Installationsanleitung.

Umweltschutz

Entsorgen Sie alte Batterien und/oder Blades/Systemkomponenten/RTMs stets gemäß der in Ihrem Land gültigen Gesetzgebung und den Empfehlungen des Herstellers.

1.1 Features

The ATCA-7365-CE is a high-performance ATCA compliant single board computer designed for demanding storage and processing applications.

The following is the list of main features:

- Dual socket Intel Xeon 5600 Series CPU
  Standard configuration ATCA-7365-xxGB-CE and ATCA-7365-xxGB-V-CE: Intel Xeon E5645 6-core 80W 2.4 GHz
  Standard configuration ATCA-7365-xxGB-L-CE: Intel Xeon E5620 4-core 80W 2.4 GHz
  DDR3 memory running at 1066 MHz
  LVDDR3 memory support (1.35V) for better thermal performance and reduced power consumption
- Intel 5520 I/O hub spanning 36 PCIe Gen2 lanes (5 Gbps)
- 4 GB onboard USB flash module assembly option with capacity up to 16GB (available upon request)
- PCIe Generation 2 with 5 Gbps
- Dual Gb Ethernet AdvancedTCA base interface
- Dual 10/1Gb Ethernet AdvancedTCA fabric interface (PICMG opt. 9 and 1)
- Additional GbE ports on faceplate and AdvancedTCA Update Channel
- Serial over LAN via AdvancedTCA base interface
- CPU and I/O virtualization support
- Power management support
- Crisis recovery for BIOS, IPMC firmware and FPGA code
- Extension slot for SATA module
- Extension slot for the PMEM (Persistent Memory) module

1.2 Standard Compliances

The product is designed to meet the following standards.

Table 1-1 Standard Compliances

Standard	Description
UL 60950-1 EN 60950-1 IEC 60950-1 CAN/CSA C22.2 No 60950-1	Legal safety requirements
CISPR 22 CISPR 24 EN 55022 EN 55024 FCC Part 15 EN 300386	EMC requirements on system level (predefined Artesyn Embedded Technologies system)
ISO 8601	Y2K compliance
PICMG 3.0[1] and 3.1	Defines mechanics, blade dimensions, power distribution, power and data connectors, and system management

1. Environmental conditions and supply voltage do not entirely follow the PICMG 3.0 but are adapted to data center application requirements.

The product has been designed to meet the directive on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS) Directive 2011/65/EU.

The following figure contains the Declaration of Conformity for ATCA-7365-CE.

Figure 1-1 Declaration of Conformity

Declaration of Conformity (DoC)

According to EN 17050-1:2004

Manufacturer's Name:	Artesyn Embedded Technologies
Manufacturer's Address:	Artesyn Embedded Technologies GmbH Lilienthalstrasse 17-19 85579 Neubiberg Germany

Declares that the following product

Product:	**ATCA Blade with Rear Transition Modules**
Model Names / Numbers:	**ATCA-7360, ATCA-7365, ATCA-7365-CE** **RTM-ATCA-7360, RTM-ATCA-7360-L** **RTM-ATCA-736X-10G, RTM-ATCA-736X-10G-SP**

in accordance with the requirements of 2004/108/EC, 2006/95/EC & 2011/65/EU and their amending directives, has been designed and manufactured to the following specifications:

EN 60950-1:2006+A12:2011

EN 55022:2010 (Class A)

EN 55024:2010

ETSI EN 300 386 V1.6.1 (2012-09)

2011/65/EU RoHS Directive

Kai Holz
Director Engineering

Issue Date: 14/May/2014

CE

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1.3 Mechanical Data

The following table provides details about the blade's mechanical data, such as dimensions and weight.

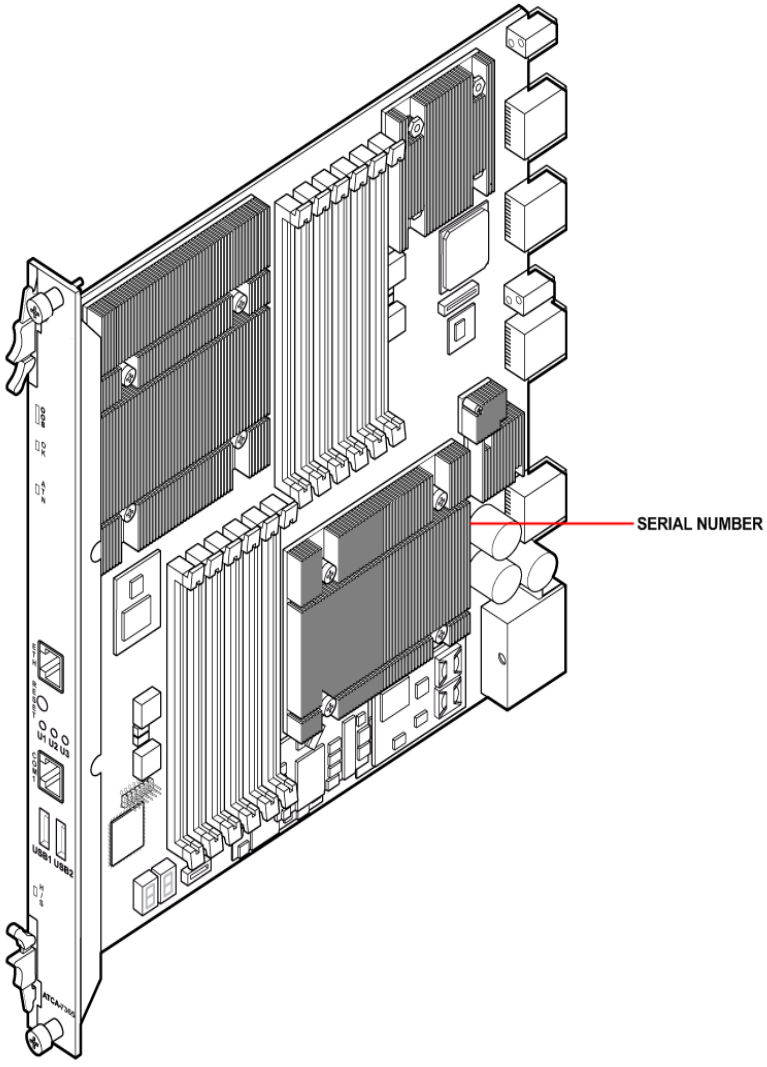
Table 1-2 Mechanical Data

Feature	Value
Dimensions (width x height x depth)	30 mm x 351 mm x 312 mm 8U form factor
Weight of blade	3.8 kg

1.4 Product Identification

The following figure shows the location of the serial number label.

Figure 1-2 Serial Number Location



1.5 Ordering Information

The following table lists the blade variants that are available upon release of this publication. Consult your local Artesyn sales representative for the availability of other variants.

Table 1-3 Blade Variants

Product Name	Description
ATCA-7365-24GB-CE	Commercial-ATCA Blade, dual Intel Xeon E5645 6-CORE (2.4 GHZ), 6X 4GB, 10G support (ROHS 6/6)
ATCA-7365-24GB-V-CE	Commercial-ATCA Blade, dual Intel Xeon E5645 6-CORE (2.4 GHZ), 6X 4GB, VGA Module, 10G support (ROHS 6/6)
ATCA-7365-24GB-L-CE	Commercial-ATCA Blade, Dual Intel Xeon E5620 QUAD-CORE (2.4 GHZ), 6X 4GB, 10G support (ROHS 6/6)

The following table lists the blade accessories that are available upon release of this publication. Consult your local sales representative for the availability of other accessories.

Table 1-4 Blade Accessories

Accessory	Description
ATCA-7360-MEM-2G	2 GB DDR3 VLP memory module for ATCA-736X product series
ATCA-7360-MEM-4G	4 GB DDR3 VLP memory module for ATCA-736X product series
ATCA-7360-MEM-8G	8 GB DDR3 VLP memory module for ATCA-736X product series
RTM-ATCA-7360	RTM for the ATCA-736X product series, 6x GBE, 2x SAS, 1x optional HDD
RTM-ATCA-7360-L	RTM for the ATCA-736X product series, 2x GBE, 2x SAS, 1x optional HDD
RTM-ATCA-7360-FC	RTM for the ATCA-736X product series, 6x GBE, 2x SAS, 2x FC
ATCA7360-HDD1-SAS	147 GB SAS HDD for the RTM-ATCA-7360 [1]
ATCA7360-HDD2-SAS	300 GB SAS HDD for the RTM-ATCA-7360 [1]
ATCA7360-HDD3-SATA	80 GB SATA HDD (ext. temp.) for the RTM-ATCA-7360 [1]
RTM-ATCA-7360-HDDKIT	Mounting kit for HDD/SSD devices used with RTM-ATCA-7360 variants, no disk (ROHS 6/6)
ATCA7360-MMOD-SATA1	32 GB on-board solid state disk at SATA for ATCA-736X product series[2]

Table 1-4 Blade Accessories (continued)

Accessory	Description
ATCA7360-MMOD-SATA2	64 GB on-board solid state disk at SATA for ATCA-736X product series[2]
ATCA7360-SFMMOD	Reset persistent memory, 16MB SRAM, 64MB Flash for the ATCA-736X product series[2]
RJ45-DSUB-ATCA7140	RJ-45 DSUB cable for the ATCA-7140, 7150, 7350, 736X
SA-BBS-WR30-7360	CD - BBS SW and WR PNE3.0 for ATCA-7360/7365

1. HDD kit option for RTM-ATCA-7360 and RTM-ATCA-7360-L

2. Persistent memory and solid state disk mutually exclusive

2.1 Unpacking and Inspecting the Blade

NOTICE

Damage of Circuits
Electrostatic discharge and incorrect blade installation and removal can damage circuits or shorten their life.
Before touching the blade or electronic components, make sure that you are working in an ESD-safe environment.

Shipment Inspection

To inspect the shipment, perform the following steps.

1. Verify that you have received all items of your shipment:
   - ATCA-7365-CE blade
   - One printed copy of *Quick Start Guide*
   - One printed copy of *Safety Notes Summary*
   - Any optional items ordered
2. Check for damage and report any damage or differences to the customer service.
3. Remove the desiccant bag shipped together with the blade and dispose of it according to your country's legislation.

The blade is thoroughly inspected before shipment. If any damage occurred during transportation or any items are missing, please contact our customer's service immediately.

2.2 Environmental and Power Requirements

In order to meet the environmental requirements, the blade has to be tested in the system in which it is to be installed.

Before you power up the blade, calculate the power needed according to your combination of blade upgrades and accessories.

2.2.1 Environmental Requirements

The environmental conditions must be tested and proven in the shelf configuration used. The conditions refer to the surrounding of the blade within the user environment. The product supports the specified temperature conditions in a shelf with airflow characteristics meeting at least the **CP-TA B.4** cooling profile.

- The environmental requirements of the blade may be further limited down due to installed accessories, such as hard disks or mezzanine modules, with more restrictive environmental requirements.
- Operating temperatures refer to the temperature of the air circulating around the blade and not to the actual component temperature.

NOTICE

Blade Damage
Blade Surface
High humidity and condensation on the blade surface causes short circuits.
Do not operate the blade outside the specified environmental limits. Make sure the blade is completely dry and there is no moisture on any surface before applying power.

Blade Overheating and Blade Damage
Operating the blade without forced air cooling may lead to blade overheating and thus blade damage.
When operating the blade, make sure that forced air cooling is available in the shelf.

Table 2-1 Environmental Requirements

Requirement	Operating	Non-Operating
Temperature	+5 °C (41 °F) to +35 °C (95 °F)	-40 °C (-40 °F) to +70 °C (158 °F) (may be further limited by installed accessories)
Temperature Change	+/- 0.25 °C/min according to NEBS Standard GR-63-CORE	+/- 0.25 °C/min
Relative Humidity	5% to 90% non-condensing according to Artesyn-internal environmental requirements	5% to 95% non-condensing according to Artesyn-internal environmental requirements
Vibration	0.1 g from 5 to 100 Hz and back to 5 Hz at a rate of 0.1 octave/minute	5-20 Hz at 0.01 g^2/Hz 20-200 Hz at -3.0 dB/octave Random 5-20 Hz at 1 m^2/Sec^3 Random 20-200 Hz at -3 m/Sec^2
Shock	Half-sine, 11 m/Sec, 30mSec/Sec^2	Blade level packaging Half-sine, 6 mSec at 180 m/Sec^2
Free Fall	-	1.0 m (packaged in blade level packaging)

During the safety qualification of this blade, the following on-board locations were identified as critical with regards to the maximum temperature during blade operation. To guarantee proper blade operation and to ensure safety, you have to make sure that the temperatures at the locations specified in the following are not exceeded. If not stated otherwise, the temperatures should be measured by placing a sensor exactly at the given locations.

Table 2-2 Critical Temperature Limits

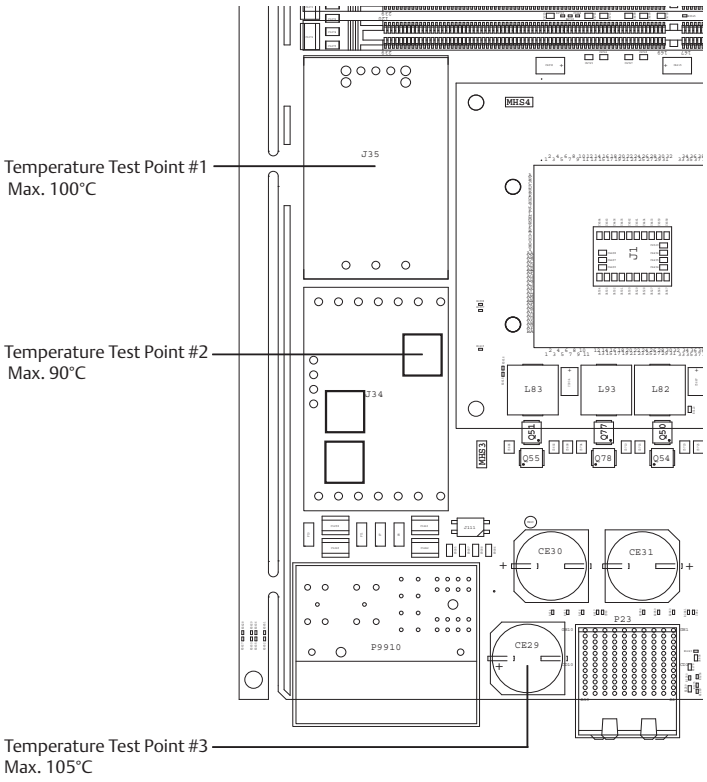
Component	Thermal Design Power	Max Case or Junction Temperature
Intel Xeon 5600 E5645 6-core	80 W	T_{jmax} = 76.2°C (junction)
Intel Xeon 5600 E5620 4-core	80 W	T_{jmax} = 77.6°C (junction)
Tylersburg IOH36 D	27.1 W	T_{cmax} = 105°C (case)
ICH10R	4.5 W	T_{cmax} = 105°C
Intel 82599 (Niantic)	8.82 W	T_{cmax} = 120°C

Table 2-2 Critical Temperature Limits (continued)

Component	Thermal Design Power	Max Case or Junction Temperature
Intel 82576 (Kawela)	2.8 W	T_{cmax} = 110°C (case)
Intel 82572EI	2.1 W (typical 1.5W)	T_{cmax} = 97°C (case)
Payload DCDC 48V/12V	21 W	
DDR3 DIMM Modules	6.9 W (estimate TS team)	85° C

For your convenience all temperature spots are shown in the figure below that provides a detailed view of the blade.

Figure 2-1 Location of Critical Temperature Spots



Note: Temperature Test Point #1 (on DC/DC Converter Module): Max. 100°C (Exact location: In the geometric middle of the heat spreader).
Temperature Test Point #2 (on Power Input Module): Max. 90°C (Exact location: On top of the transformer).
Temperature Test Point #3 (on Hold-Up Capacitor): Max. 105°C

If you integrate the blade in your own system please contact your local sales Artesyn representative for further safety information.

2.2.2 Power Requirements

The blade's power requirements depend on the installed hardware accessories. If you want to install accessories on the blade, the load of the respective accessory has to be added to that of the blade. In the following table you will find typical examples of power requirements with and without accessories installed. For information on the accessories' power requirements, refer to the documentation delivered together with the respective accessory or consult your local Artesyn representative for further details.

Table 2-3 Power Requirements

Characteristic	Value
Rated Voltage	-48 VDC
Operating Voltage	-38.4 VDC to -57.6 VDC
Maximum power consumption of ATCA-7365-CE (with RTM-ATCA-7360 including a SAS HDD)	300 W (typical 240 W)
Maximum power consumption of ATCA-7365-CE (without RTM-ATCA-7360)	280 W (typical 220 W)

The blade provides two independent power inputs according to the AdvancedTCA Specification. Each input has to be equipped with an additional fuse of maximum 90A located either in the shelf where the blade is installed or the power entry module (PEM).

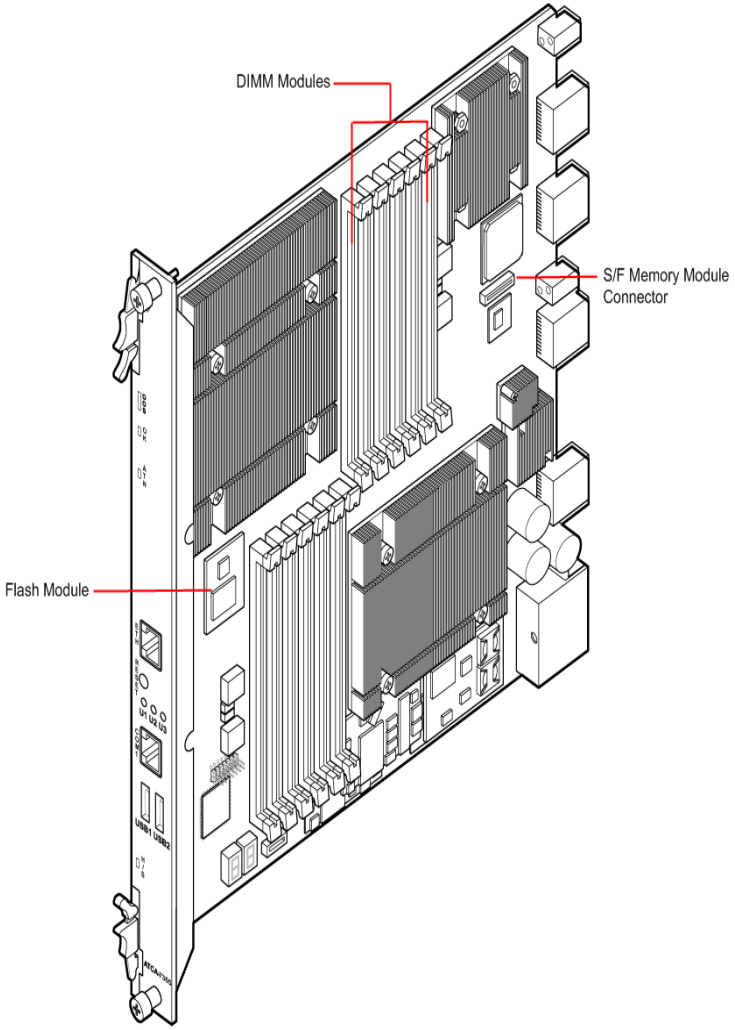
The power consumption has been measured using specific boards in a configuration considered to represent the worst-case (with RTM-ATCA-7360 and SAS HDD, maximum memory population, USB-Flash, SF-MEM persistent memory module) and with software simultaneously exercising as many functions and interfaces as possible. This includes a particular load software provided by Intel designed to stress the processors to reach their theoretical maximum power specification.

Any difference in the system configuration or the software executed by the processors may affect the actual power dissipation. Depending on the actual operating configuration and conditions, customers may see slightly higher power dissipation, or it may even be significantly lower. There is also a dependency on the batch variance of the major components like the processor and DIMMs used. Hence, Artesyn does not represent or warrant that measurement results of a specific board provide guaranteed maximum values for a series of boards.

2.3 Blade Layout

The following figure shows the location of components on the ATCA-7365-CE blade.

Figure 2-2 ATCA-7365-CE Blade Layout



2.4 Switch Settings

The blade provides the configuration switches SW1, SW2, SW3, and SW4.

NOTICE

Blade Malfunction
Switches marked a “Reserved” may carry production-related functions and may cause the blade to malfunction if their setting is changed.
Therefore, do not change settings of switches marked as “Reserved”. The setting of switches which are not marked as “Reserved” has to be checked and changed before blade installation.

Blade Damage
Setting/resetting the switches during operation can cause blade damage.
Therefore, check and change switch settings before you install the blade.

For normal operation, all switches must be OFF. Switches are used only for repair, manual maintenance and critical crisis recovery. For remote maintenance and in order that all firmware upgrade features through IPMC are available, all switches must be in their default OFF position and are controlled through IPMC.

Table 2-4 Switch Settings

Switch	Description
SW1-1	Default Boot-Flash (BIOS) write protection OFF: Write-enabled (default) ON: Write-protected
SW1-2	Recovery Boot-Flash (BIOS) write protection OFF: Write-enabled (default) ON: Write-protected
SW1-3	TSOP or debug-socket SPI boot select OFF: Boot from TSOP SPI flash (either Default/Recovery) (default) ON: Boot from debug socket SPI flash
SW1-4	ICH10 GPIO33-Pinstrap: SPI Flash Descriptor Security Override Strap and ME disable if sampled LOW OFF: No SPI Flash Descriptor security override and ME working in S0/S1 (default) ON: Flash security descriptor and ME disabled (for debugging only)
SW2-1	Serial Line #1 and #2 Routing OFF: FPGA-COM#1 to faceplate, FPGA-COM#2 to RTM (default) ON: FPGA-COM#1 to RTM, FPGA-COM#2 to faceplate Note: IPMC COM1/2 routing selection has precedence. For details, see *Serial Output Commands* on page 238.
SW2-2	IPMC Debug Console Routing OFF: IPMC debug console at 3-pin header (default) ON: IPMC debug console at faceplate instead of FPGA COM
SW2-3	FPGA-Bitstream PROM selection OFF: FPGA loads from default Bitstream PROM ON: FPGA loads from Recovery Bitstream PROM
SW2-4	PECI Master selection OFF: IPMC is PECI master ON: ICH10 is PECI master
SW3-1	Enable manual “Default SPI Boot Flash” / “Recovery SPI Boot Flash” selection OFF: IPMI selects boot flash (default) ON: SW3-2 selects Boot Flash

Table 2-4 Switch Settings (continued)

Switch	Description
SW3-2	SW3-2 controls boot flash selection if SW3-1 is set to ON OFF: Boot from "Default Boot Flash" device (default) ON: Boot from "Recovery Boot Flash" device
SW3-3	Enable faceplate (Front board and RTM) reset push button OFF: Reset push button enabled (default) ON: Reset push button disabled
SW3-4	ICH10 TCO Timer system reboot feature OFF: ICH10 TCO Timer system reboot feature enabled (default) ON: ICH10 will disable the TCO Timer system reboot feature
SW4-1	Reserved OFF: Default
SW4-2	ICH10 TCO Timer system reboot feature OFF: ICH10 TCO Timer system reboot feature enabled (default) ON: system is strapped to the "No Reboot" mode (ICH10 will disable the TCO Timer system reboot feature).
SW4-3 and SW4-4	Load BIOS default settings OFF, OFF: Normal operation OFF, ON: Load BIOS default from IPMI Boot Parameter DEFAULT area ON, OFF: Reserved ON, ON: Status Codes to COM

2.5 Installing the Blade Accessories

The following additional components are available for the blade:

- DIMM memory modules
- PMEM (persistent memory) module
- SATA module
- USB flash module
- Rear transition modules

They are described in detail in the following sections. For order numbers refer to section *Ordering Information* on page 42.

2.5.1 DIMM Memory Modules

The blade provides up to 12 memory slots for main memory DIMM modules. You may install and/or remove DIMM memory modules in order to match the main memory size to your needs. The corresponding installation/removal procedures are described in this section.

The location of the DIMM Memory Modules are shown in Figure 2-2 on page 51.

When installing DIMM memory modules, the DIMM sockets farthest away on each memory channel from the CPU device need to be populated first. Only qualified DDR3 DIMMs (Dual Ranked RDIMM) are allowed. The reason is the thermal limit/budget of the blade and the high variation of the power consumptions of different DIMMM types. For thermal reasons, no 4-rank DIMMs and no dual-Die DIMM are allowed.

ATCA-7365-CE supports low-voltage DDR3 memory. This is available upon request.

DIMM modules used within one channel must be based on the same memory technology. To achieve proper functionality in all use cases, it is highly recommended to insert only one type of memory module from one vendor across all DIMM slots on the board. If mixing different types of DIMMs or using the same type of DIMM from different vendors on one blade, then the full functionality in all cases cannot be guaranteed.

NOTICE

Damage of Circuits
Electrostatic discharge and incorrect module installation and removal can damage circuits or shorten their life.
Before touching the module or electronic components, make sure that you are working in an ESD-safe environment.

Installation Procedure

To install a DIMM module, proceed as follows:

1. Remove the blade from system as described in *Installing and Removing the Blade* on page 59.
2. Open the locks of memory module socket.
3. Press module carefully into the socket.
   As soon as the memory module has been fully inserted, the locks automatically close.
4. If applicable, repeat steps 2 to 3 to install further modules.

NOTICE

Damage of Circuits
Electrostatic discharge and incorrect module installation and removal can damage circuits or shorten their life.
Before touching the module or electronic components, make sure that you are working in an ESD-safe environment.

Removal Procedure

To remove a DIMM module, proceed as follows:

1. Remove the blade from system as described in *Installing and Removing the Blade* on page 59.
2. Open the locks of socket at both sides.
   The memory module is automatically lifted up.
3. Remove module from socket.
4. Repeat steps 2 to 3 in order to remove further memory modules.

2.5.2 PMEM and SATA Module

The PMEM/SATA extension slot allows assembly of either a PMEM or SATA module which are available as upgrade kits for ATCA-7365-CE. PMEM module consists of an SRAM and a flash memory. The SRAM has a capacity of up to 16 MB and can be used as persistent memory, i.e. a memory that holds up the contents during reset. The flash memory has a capacity of up to 64 MB organized as two memory banks. The S/F memory module connects to the blade's PCI subsystem. It can be configured via an FPGA register.

The SATA module consists of a Solid State Disc of up to 128 GB and a SATA controller and connects physically to ICH10 SATA Port #5.

The extension module is mechanically fastened to the blade with two screws. The location of the two corresponding mounting holes as well as the S/F memory module connector is shown in Figure 2-2 on page 51.

The PMEM and SATA module are accessory kits and are not part of the default ATCA-7365.The following procedure describes the steps to install/remove the PMEM/SATA module.

Installation Procedure

To install a PMEM/SATA module, proceed as follows:

NOTICE

Damage of Circuits
Electrostatic discharge and incorrect module installation and removal can damage circuits or shorten their life.
Before touching the module or electronic components, make sure that you are working in an ESD-safe environment.

1. Remove the blade from the system as described in *Installing and Removing the Blade* on page 59.
2. Plug the PMEM/SATA module on the blade so that the module's standoffs fit in the blade's mounting holes.

3. Fasten the PMEM/SATA module to the blade using the two screws that previously had fixed the S/F memory module to the blade.
4. Reinstall the blade into the system as described in *Installing and Removing the Blade* on page 59.
   The additional resource (either memory or SATA SSD) will be detected automatically during the boot-up sequence.

Removal Procedure

To remove a PMEM/SATA module, proceed as follows:

NOTICE

Damage of Circuits
Electrostatic discharge and incorrect module installation and removal can damage circuits or shorten their life.
Before touching the module or electronic components, make sure that you are working in an ESD-safe environment.

1. Remove the blade from the system as described in *Installing and Removing the Blade* on page 59.
2. Remove the two screws holding the PMEM/SATA module.
3. Remove the PMEM/SATA module from the blade.
4. Reinstall the blade into the system as described in *Installing and Removing the Blade* on page 59.

2.5.3 USB 2.0 Flash Module

The blades provides a USB 2.0 flash module with a capacity of 4 GB or 16 GB. The corresponding removal/installation procedures are described in this section.

The location of the USB 2.0 Flash Module is shown in Figure 2-2 on page 51.

NOTICE

Damage of Circuits
Electrostatic discharge and incorrect module installation and removal can damage circuits or shorten their life.
Before touching the module or electronic components, make sure that you are working in an ESD-safe environment.

Removal Procedure

To remove a USB flash module, proceed as follows:

1. Remove blade from system as described in *Removing the Blade* on page 63.
2. Remove the screw on the left side of the flash module (see figure Figure 2-2 on page 51).
3. Lift the flash module from the socket.

Installation Procedure

To install a USB flash module, proceed as follows:

1. Remove blade from system as described in *Removing the Blade* on page 63.
2. Insert new flash module in socket (see figure Figure 2-2 on page 51).
3. Tighten the screw on the left side of the flash module.

2.6 Installing and Removing the Blade

The blade is fully compatible to the AdvancedTCA standard and is designed to be used in AdvancedTCA shelves.

The blade can be installed in any AdvancedTCA node slot. Do not install it in an AdvancedTCA hub slot.

NOTICE

Damage of Circuits
Electrostatic discharge and incorrect blade installation and removal can damage circuits or shorten their life.
Before touching the blade or electronic components, make sure that you are working in an ESD-safe environment.

Blade Malfunctioning
Incorrect blade installation and removal can result in blade malfunctioning.
When plugging the blade in or removing it, do not press on the faceplate but use the handles.

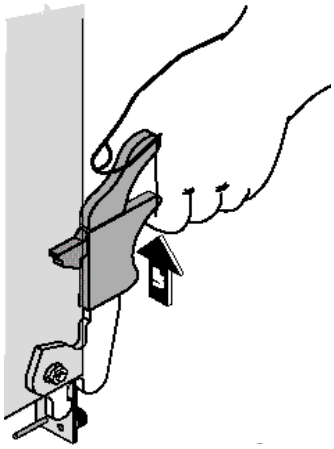
2.6.1 Installing the Blade

To install the blade into an AdvancedTCA shelf, proceed as follows.

Installation Procedure

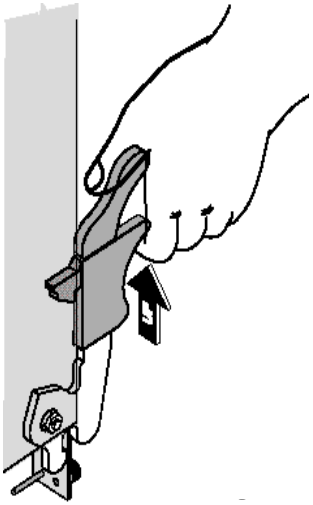
The following procedure describes the installation of the blade. It assumes that your system is powered on. If your system is not powered on, you can disregard the blue LED and skip the respective step. In this case, it is purely a mechanical installation.

1. Ensure that the top and bottom ejector handles are in the outward position by squeezing the lever and the latch together.



2. Insert blade into the shelf by placing the top and bottom edges of the blade in the card guides of the shelf. Ensure that the guiding module of shelf and blade are aligned properly.
3. Apply equal and steady pressure to the blade to carefully slide the blade into the shelf until you feel resistance. Continue to gently push the blade until the blade connectors engage.
4. Squeeze the lever and the latch together and hook the lower and the upper handle into the shelf rail recesses.

5. Fully insert the blade and lock it to the shelf by squeezing the lever and the latch together and turning the handles towards the faceplate.



If your shelf is powered on, as soon as the blade is connected to the backplane power pins, the blue LED is illuminated.
When the blade is completely installed, the blue LED starts to blink. This indicates that the blade announces its presence to the shelf management controller.

If an RTM is connected to the front blade, make sure that the handles of both the RTM and the front blade are closed in order to power up the blade's payload.

6. Wait until the blue LED is switched off, then tighten the faceplate screws which secure the blade to the shelf.
   The switched off blue LED indicates that the blade's payload has been powered up and that the blade is active.
7. Connect cables to the faceplate, if applicable.

2.6.2 Removing the Blade

This section describes how to remove the blade from an AdvancedTCA system.

NOTICE

Damage of Circuits
Electrostatic discharge and incorrect blade installation and removal can damage circuits or shorten their life.
Before touching the blade or electronic components, make sure that you are working in an ESD-safe environment.

Blade Malfunctioning
Incorrect blade installation and removal can result in blade malfunctioning.
When plugging the blade in or removing it, do not press on the faceplate but use the handles.

Removal Procedure

The following procedure describes how to remove the blade from a system. It assumes that the system is powered on. If the system is not powered on, you can disregard the blue LED and skip the respective step. In that case, it is purely a mechanical procedure.

1. Unlatch the lower handle by squeezing the lever and the latch together and turning the handle outward just enough to unlatch the handle from the faceplate. Do not rotate the handle fully outward.
   The blue LED blinks indicating that the blade power-down process is ongoing.
2. Wait until the blue LED is illuminated permanently, then unlatch the upper handle and rotate both handles fully outward.

If the LED continues to blink, a possible reason may be that the upper layer software rejected the blade extraction request.

NOTICE

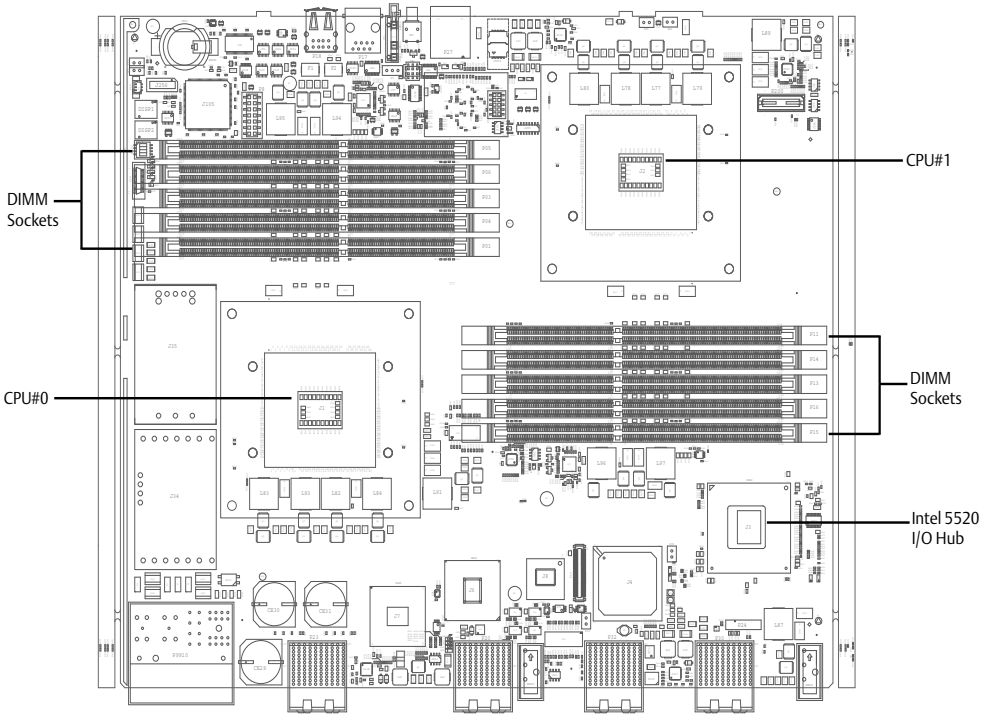
Data Loss
Removing the blade with the blue LED still blinking causes data loss.
Wait until the blue LED is permanently illuminated, before removing the blade.

3. Remove the faceplate cables, if applicable.
4. Unfasten the screws of the faceplate until the blade is detached from the shelf.
5. Remove the blade from the shelf.

3.1 Mechanical Layout

The following graphic illustrates the mechanical layout of the blade.

Figure 3-1 Mechanical Layout



3.2 Faceplate

The following figure illustrates the connectors, keys and LEDs available on the faceplate.

Figure 3-2 Faceplate

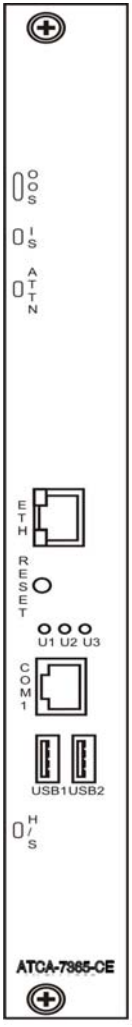
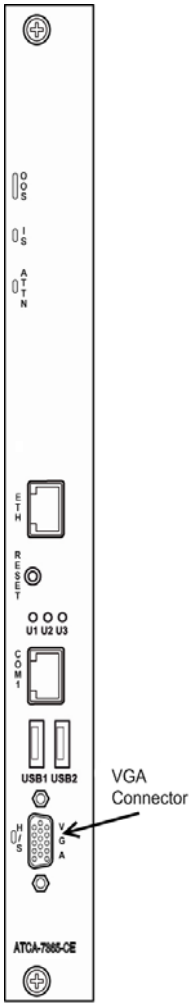


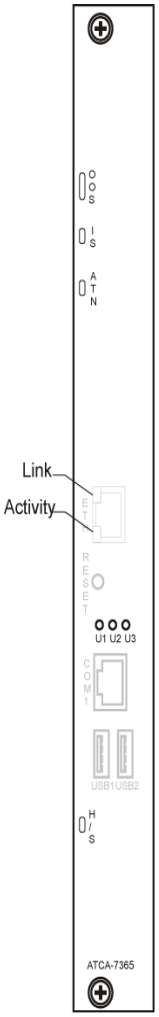
Figure 3-3 Faceplate (with VGA Module)



3.2.1 LEDs

The following figure illustrates all LEDs available on the faceplate.

Figure 3-4 Location of Faceplate LEDs



The meaning of these LEDs is described in the following table.

Table 3-1 FacePlate LEDs

LED	Description
OOS	Out Of Service This LED is multicolored (red/amber) and is programmable through IPMC. Its default color is red and its local control state (on or off) reflects the payload power state (on or off). It permits override control by higher layer software, such as middle ware or applications, as specified in PICMG 3.0 specification.
IS	Payload Power Status This LED is multicolored (green/red/amber) and is programmable through IPMC. Its default color is green and its local control state is off. It permits override control by higher layer software, such as middle ware or applications, as specified in PICMG 3.0 specification.
ATN	Attention This LED has amber color and is programmable through IPMC. Its local control state is off. It permits override control by higher layer software, such as middle ware or applications, as specified in PICMG 3.0 specification.
ETH Status LEDs	The Ethernet connector provides two status LEDs Link (upper) Green: Link is available Off: No link Activity (lower) Yellow: Activity Off: No activity
U1, U2	Base interface activity is visualized via FPGA LEDs U1 and U2
U3	User LED, selectable color via FPGA register. Colors: red, green, orange

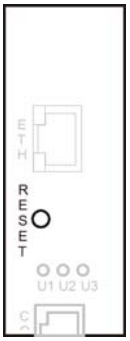
Table 3-1 FacePlate LEDs (continued)

LED	Description
H/S	FRU State Machine During blade installation: Permanently blue: On-board IPMC powers up Blinking blue: Blade communicates with shelf manager OFF: Blade is active During blade removal: Blinking blue: Blade notifies shelf manager of its desire to deactivate Permanently blue: Blade is ready to be extracted

3.2.2 Keys

The blade provides one faceplate reset key.

Figure 3-5 Location of FacePlate Reset Key



On pressing it, a hard reset is triggered and all attached on-board devices are reset.

You cannot reset the IPMC via this key.

3.2.3 Connectors

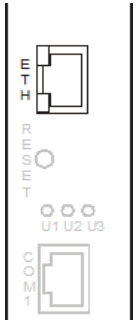
The blade provides the following connectors at its faceplate:

- 1x Ethernet
- 1x Serial
- 2x USB
- VGA Connector (supported on ATCA-7365-24GB-V-CE)

3.2.3.1 Ethernet Connector

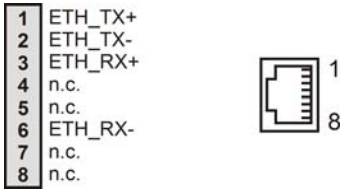
The blade provides one Ethernet 1000Base-T interface connector at its faceplate. It is intended for blade configuration and constitutes, besides the two AdvancedTCA Base interfaces, a third Ethernet interface to access the blade. The location of the Ethernet connector is shown in the following figure.

Figure 3-6 Location of Ethernet Connector



The pinout of the connector is as follows.

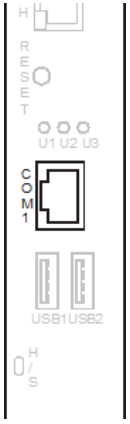
Figure 3-7 Ethernet Interface Connectors Pinout



3.2.3.2 Serial Interface Connector

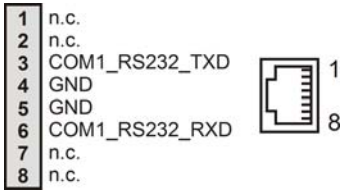
The blade provides one RS-232 serial interface connector at its faceplate. It is of type RJ-45 and corresponds to the physical serial interface port 1. By default, the BIOS maps this interface to the serial interface COM1. The on-board switch 2-1 allows to swap COM1 with COM2 and thus make COM2 accessible via the faceplate connector instead. Note that the BIOS serial redirection feature uses COM1 as access interface. Therefore swapping the serial interfaces via SW2-1 also changes the serial connector that you need to access to make use of the serial redirection feature. The location of the connector is shown in the following figure.

Figure 3-8 Location of Serial Connector



The pinout of the serial interface connector is shown below.

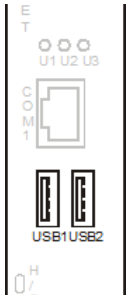
Figure 3-9 Serial Interface Connector Pinout



3.2.3.3 USB Connectors

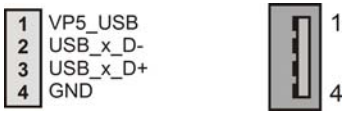
The blade provides two USB connectors at its faceplate. They are compliant to the USB 2.0 standard and correspond to the blade's USB interfaces 3 and 4. Their location is shown in the following figure.

Figure 3-10 Location of USB Connectors



The pinout of each USB connector is given in the following.

Figure 3-11 USB Connector Pinout



NOTICE

Exceeding the maximum USB current rating of 500mA per Port will result in ATCA-7360 protecting itself through a controlled board shutdown.

3.2.3.4 VGA-7360 Module Connector

The variants of ATCA-7365 support the VGA-7360 module. For more information, refer to *VGA Module* on page 152.

Table 3-2 VGA-7360 Module Connector Pinout

Pin	Signal	Pin	Signal
1	GND	2	GND
3	+1.8V	4	PCIE_TX+
5	+1.8V	6	PCIE_TX-
7	GND	8	GND
9	+3.3V	10	PCIE_RX+
11	+3.3V	12	PCIE_RX-
13	GND	14	GND
15	+5V	16	PCIE_CLK100MHz+
17	PCIE_RST#	18	PCIE_CLK100MHz-
19	GND	20	GND

Table 3-3 FacePlate VGA Connector Signals

Pin	Signal	Pin	Signal	Pin	Signal
11	-	6	GND	1	RED
12	SDA	7	GND	2	GREEN
13	HSYNC	8	GND	3	BLUE
14	VSYNC	9	+5V	4	-
15	SCLK	10	GND	5	GND

NOTICE

Ensure that the display devices that are permanently connected to the VGA interface provide a fire enclosure according to the IEC/EN/UL/CSA 60950-1 requirements.
All other devices that are connected only for service purposes to the VGA interface needs supervision during operation and must be disconnected after maintenance.

3.3 On-board Connectors

The blade provides the following on-board connectors:

- PMEM/SATA module connector
- USB flash module connector

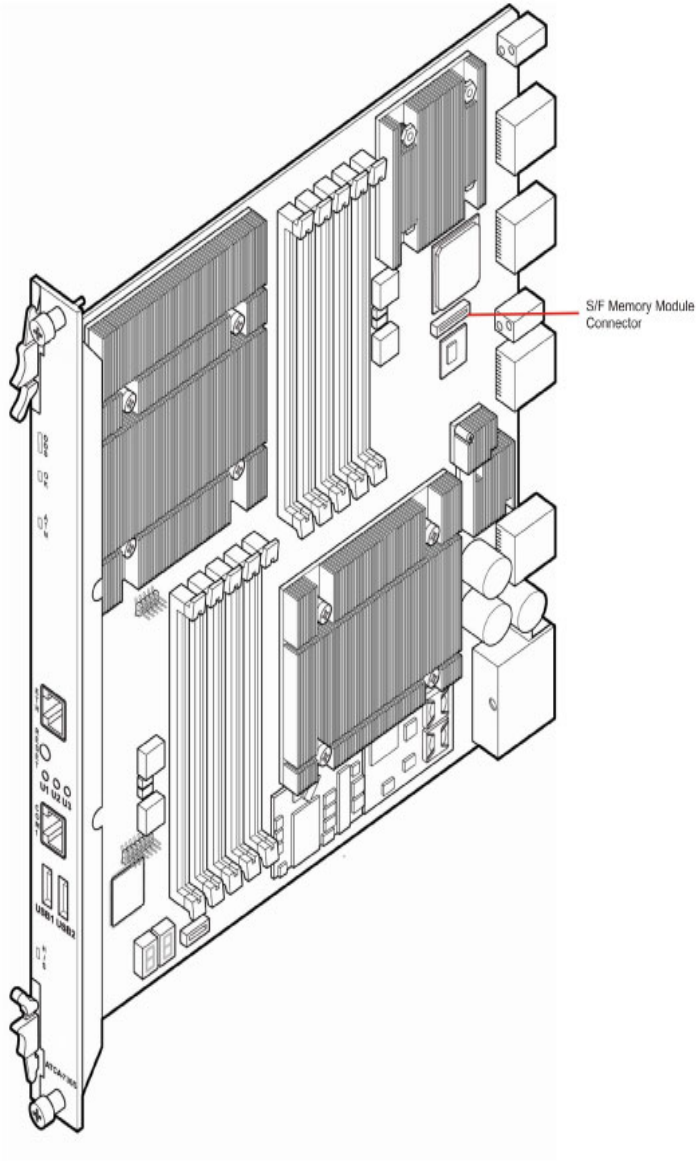
3.3.1 PMEM/SFMEM Module Connector

The PMEM/SFMEM Module connects to the blade through a connector that carries the following types of signals:

- PCI interface signals
- I2C signals for connection with on-board IDROM device
- Four configuration pins used for memory configuration
- 1 SATA port connection (ICH10 port #5)
- Power supply 5V and 3.3V

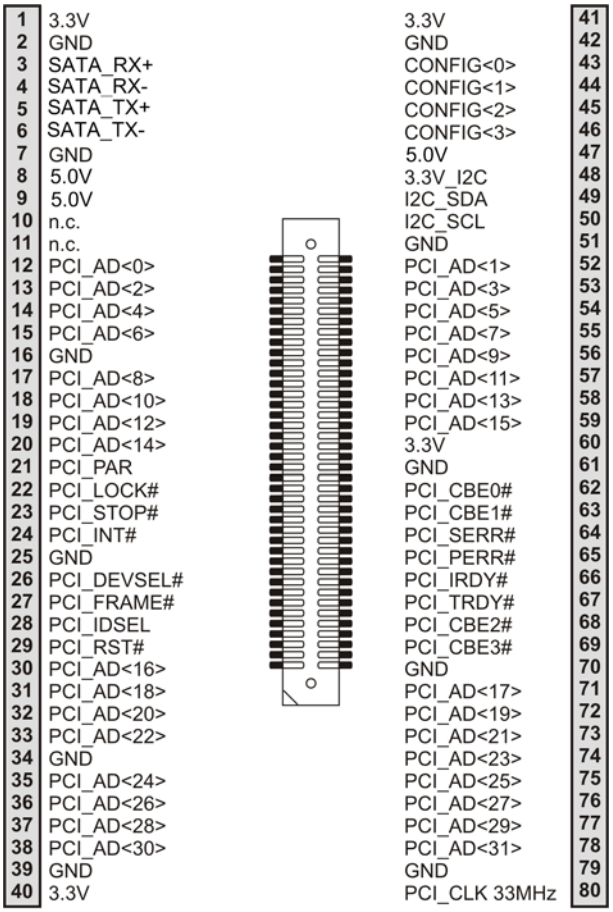
The location of the PMEM/SFMEM module connector is illustrated in the following figure.

Figure 3-12 Location ofPMEM/SFMEM Module Connector



The pinout of this connector is illustrated in the following figure.

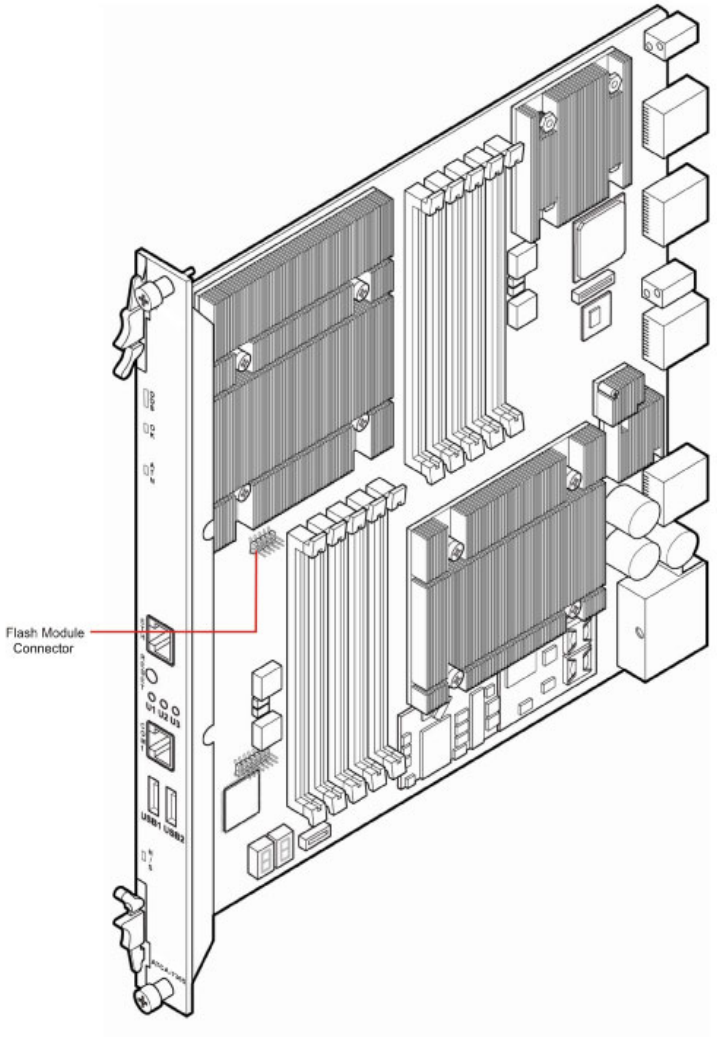
Figure 3-13 PMEM/SATA Module Connector Pinout



3.3.2 USB Flash Module Connector

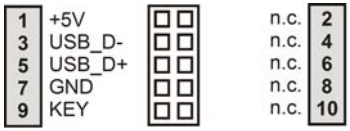
The location of the flash memory module connector is illustrated in the following figure.

Figure 3-14 Location of USB Flash Module Connector



You can find the pin assignment of the flash connector in the following figure.

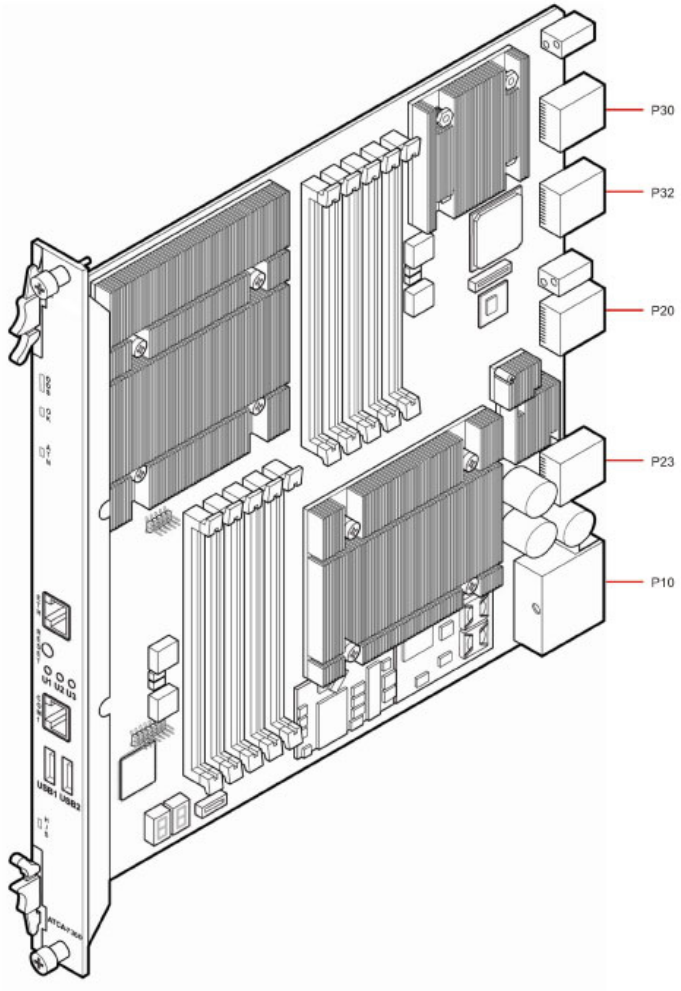
Figure 3-15 USB Flash Module Connector Pin Assignment



3.4 AdvancedTCA Backplane Connectors

The AdvancedTCA backplane connectors reside in the three zones 1 to 3 as specified by the AdvancedTCA standard and are called P10, P20 and 23 and P30 and 32. The pinouts of all these connectors are given in this section.

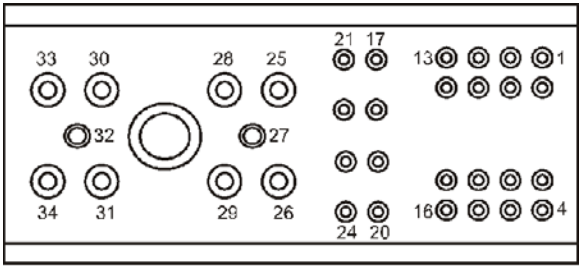
Figure 3-16 Location of AdvancedTCA Connectors



The connector residing in zone 1 is called P10 and carries the following signals:

- Power feed for the blade (VM48_x_CON and RTN_x_CON)
- Power enable (ENABLE_x)
- IPMB bus signals (IPMB0_x_yyy)
- Geographic address signals (HAx)
- Ground signals (SHELF_GND and GND)
- Reserved signals

Figure 3-17 P10 Backplane Connector Pinout



1	Reserved	18	n.c.
2	Reserved	19	n.c.
3	Reserved	20	n.c.
4	Reserved	21	n.c.
5	HA0	22	n.c.
6	HA1	23	n.c.
7	HA2	24	n.c.
8	HA3	25	SHELF_GND
9	HA4	26	GND
10	HA5	27	ENABLE_B
11	HA6	28	RTN_A_CON
12	HA7	29	RTN_B_CON
13	IPMB0_A_SCL	30	n.c.
14	IPMB0_A_SDA	31	n.c.
15	IPMB0_B_SCL	32	ENABLE_A
16	IPMB0_B_SDA	33	VM48_A_CON
17	n.c.	34	VM48_B_CON

Zone 2 contains the two connectors P20 and P23. They carry the following types of signals:

- Telecom clock signals (CLKx_)
- Base interface signals (BASE_)

- SAS update channel
- 100Base-BX update channel

Some of the pins provided by P20 and P23 are defined as optional in the AdvancedTCA specification and are unused on the blade. If the AdvancedTCA specification defines these signals as input signals, they are terminated on the blade and marked as "TERM_" in the following pinouts. In all other cases the pins are unconnected and consequently marked as "n.c.".

The pinouts of P20 and P23 are as follows.

Figure 3-18 P20 Backplane Connector Pinout - Rows A to D

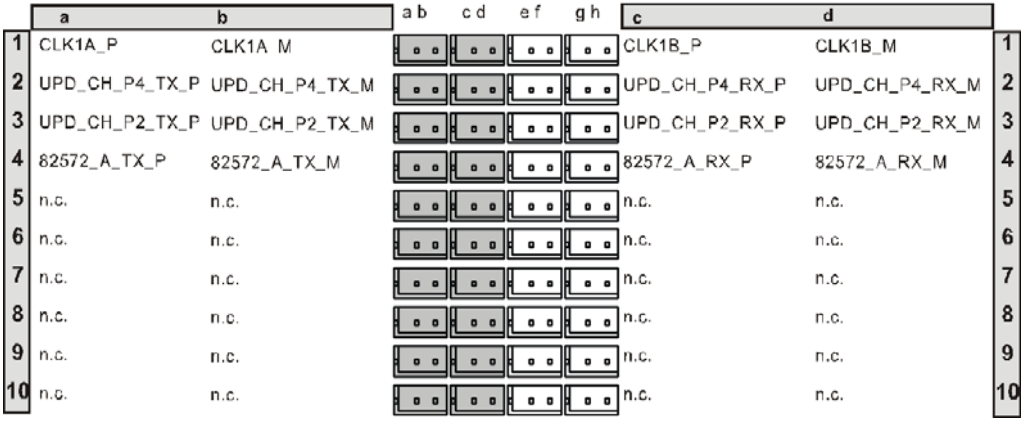
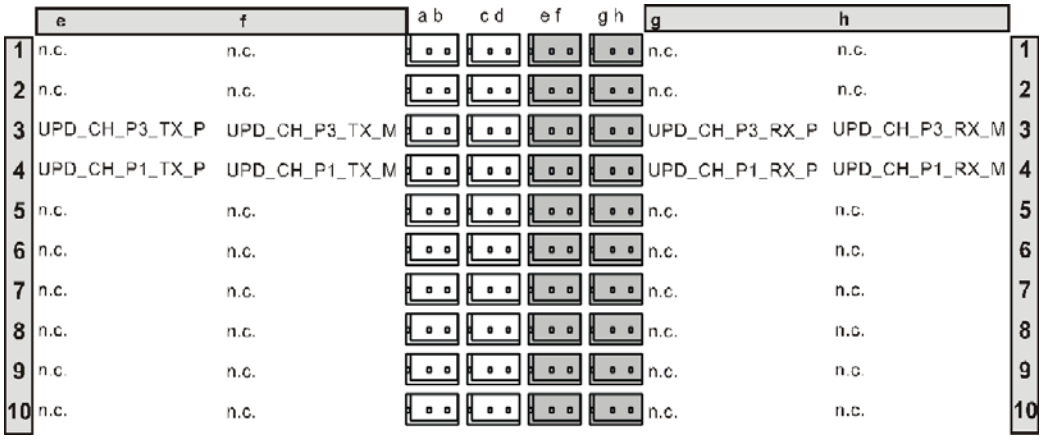
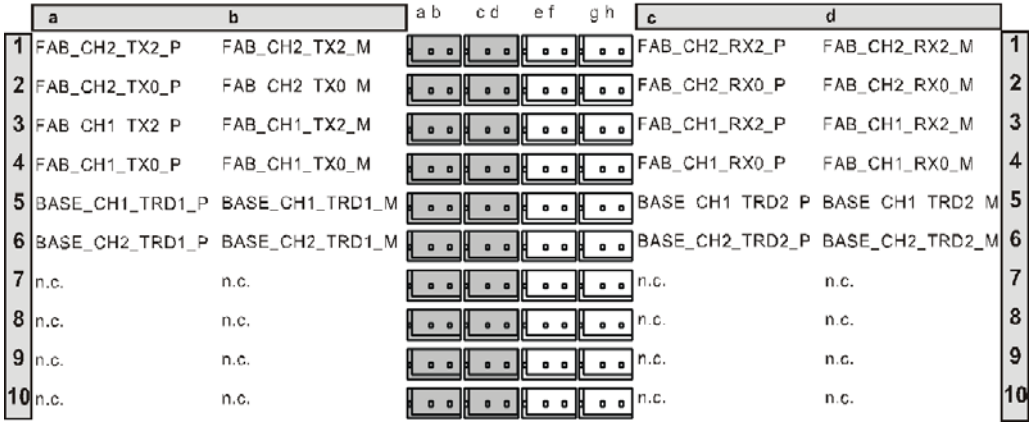


Figure 3-19 P20 Backplane Connector Pinout - Rows E to H



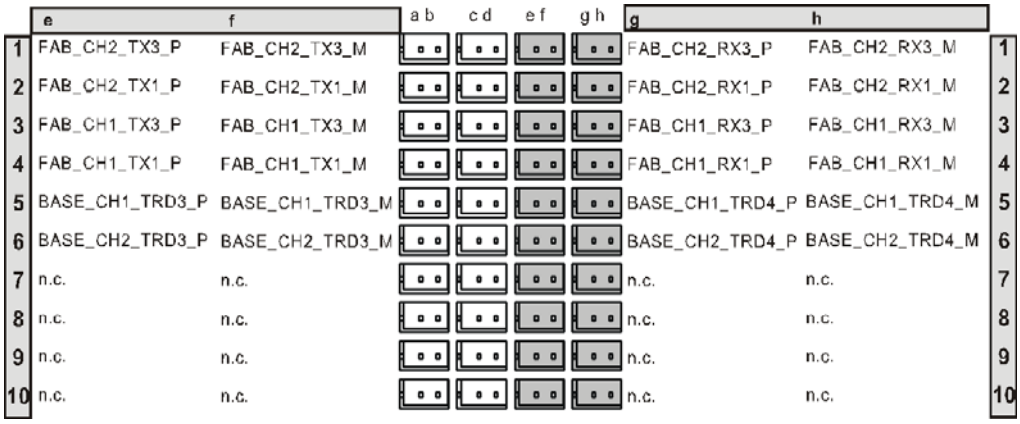
	e	f	ab cd ef gh	g	h	
1	n.c.	n.c.		n.c.	n.c.	1
2	n.c.	n.c.		n.c.	n.c.	2
3	UPD_CH_P3_TX_P	UPD_CH_P3_TX_M		UPD_CH_P3_RX_P	UPD_CH_P3_RX_M	3
4	UPD_CH_P1_TX_P	UPD_CH_P1_TX_M		UPD_CH_P1_RX_P	UPD_CH_P1_RX_M	4
5	n.c.	n.c.		n.c.	n.c.	5
6	n.c.	n.c.		n.c.	n.c.	6
7	n.c.	n.c.		n.c.	n.c.	7
8	n.c.	n.c.		n.c.	n.c.	8
9	n.c.	n.c.		n.c.	n.c.	9
10	n.c.	n.c.		n.c.	n.c.	10

Figure 3-20 P23 Backplane Connector Pinout - Rows A to D



	a	b	ab cd ef gh	c	d	
1	FAB_CH2_TX2_P	FAB_CH2_TX2_M		FAB_CH2_RX2_P	FAB_CH2_RX2_M	1
2	FAB_CH2_TX0_P	FAB CH2 TX0 M		FAB_CH2_RX0_P	FAB_CH2_RX0_M	2
3	FAB CH1 TX2 P	FAB_CH1_TX2_M		FAB_CH1_RX2_P	FAB_CH1_RX2_M	3
4	FAB_CH1_TX0_P	FAB_CH1_TX0_M		FAB_CH1_RX0_P	FAB_CH1_RX0_M	4
5	BASE_CH1_TRD1_P	BASE_CH1_TRD1_M		BASE CH1 TRD2 P	BASE CH1 TRD2 M	5
6	BASE_CH2_TRD1_P	BASE_CH2_TRD1_M		BASE_CH2_TRD2_P	BASE_CH2_TRD2_M	6
7	n.c.	n.c.		n.c.	n.c.	7
8	n.c.	n.c.		n.c.	n.c.	8
9	n.c.	n.c.		n.c.	n.c.	9
10	n.c.	n.c.		n.c.	n.c.	10

Figure 3-21 P23 Backplane Connector Pinout - Rows E to H

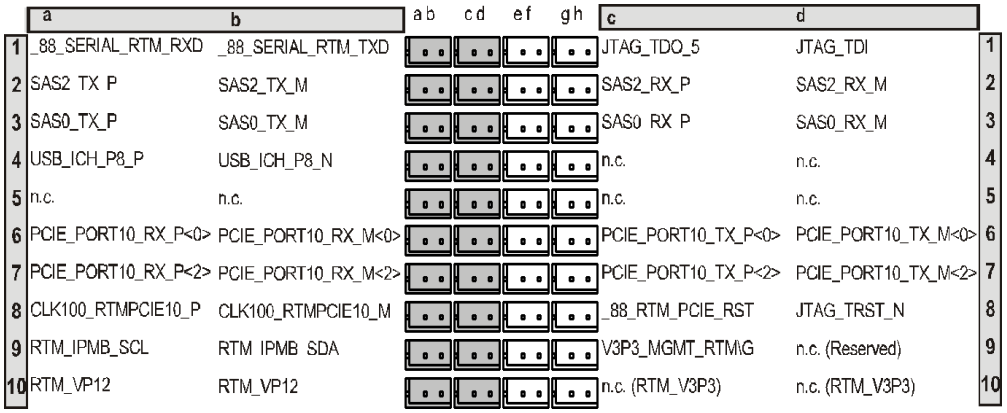


Zone 3 contains the two connectors P30 and P32. They are used to connect an RTM to the blade and carry the following signals:

- Serial (RS232_x_yyyy)
- Serial ATA (SATAx_yyy)
- USB (USBxy)
- PCI Express (PCIEx_yyy)
- IPMI (IPMB1_xxx, ISMB_xxx)
- Power (VP12_RTM, V3P3_RTM, VP5_RTM)

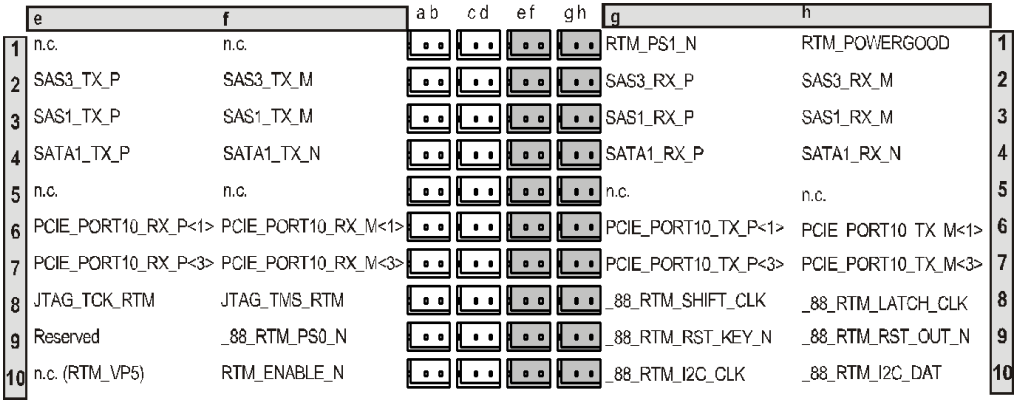
- SAS Update channels
- General control signals (BD_PRESENTx, RTM_PRSNT_N, RTM_RST_KEY-, RTM_RST-)

Figure 3-22 P30 Backplane Connector Pinout - Rows A to D



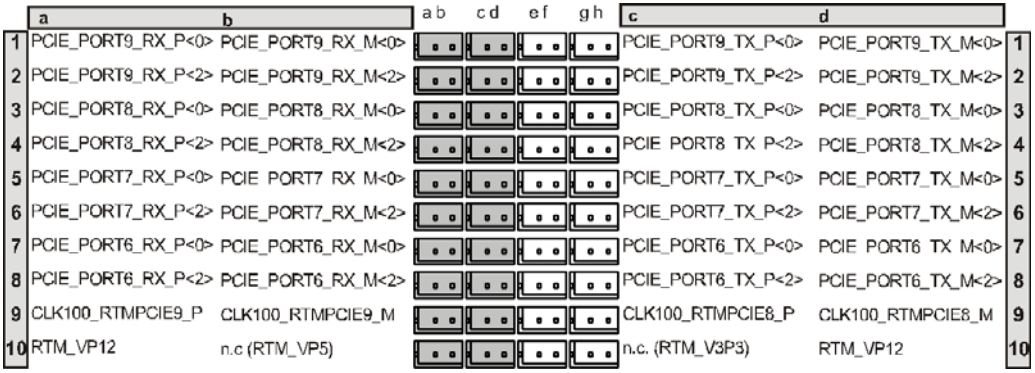
	a	b	ab cd ef gh	c	d	
1	_88_SERIAL_RTM_RXD	_88_SERIAL_RTM_TXD		JTAG_TDO_5	JTAG_TDI	1
2	SAS2 TX P	SAS2_TX_M		SAS2_RX_P	SAS2_RX_M	2
3	SAS0_TX_P	SAS0_TX_M		SAS0 RX P	SAS0_RX_M	3
4	USB_ICH_P8_P	USB_ICH_P8_N		n.c.	n.c.	4
5	n.c.	n.c.		n.c.	n.c.	5
6	PCIE_PORT10_RX_P<0>	PCIE_PORT10_RX_M<0>		PCIE_PORT10_TX_P<0>	PCIE_PORT10_TX_M<0>	6
7	PCIE_PORT10_RX_P<2>	PCIE_PORT10_RX_M<2>		PCIE_PORT10_TX_P<2>	PCIE_PORT10_TX_M<2>	7
8	CLK100_RTMPCIE10_P	CLK100_RTMPCIE10_M		_88_RTM_PCIE_RST	JTAG_TRST_N	8
9	RTM_IPMB_SCL	RTM IPMB SDA		V3P3_MGMT_RTM\G	n.c. (Reserved)	9
10	RTM_VP12	RTM_VP12		n.c. (RTM_V3P3)	n.c. (RTM_V3P3)	10

Figure 3-23 P30 Backplane Connector Pinout - Rows E to H



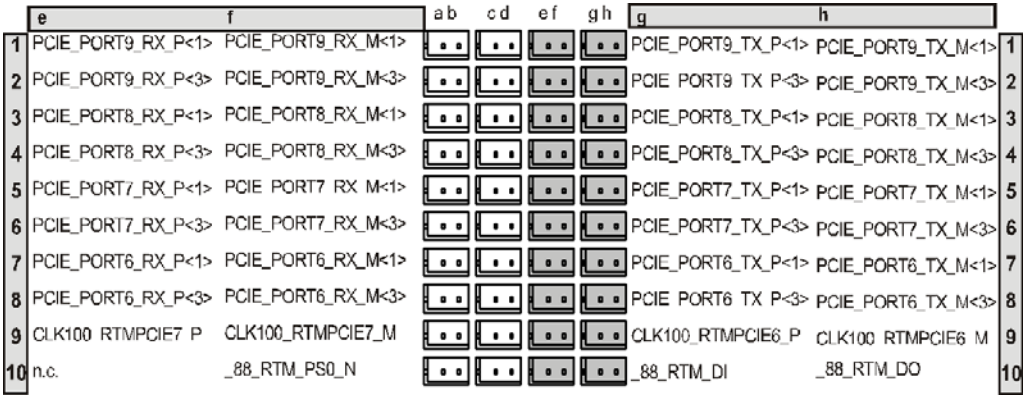
	e	f	ab cd ef gh	g	h	
1	n.c.	n.c.		RTM_PS1_N	RTM_POWERGOOD	1
2	SAS3_TX_P	SAS3_TX_M		SAS3_RX_P	SAS3_RX_M	2
3	SAS1_TX_P	SAS1_TX_M		SAS1_RX_P	SAS1_RX_M	3
4	SATA1_TX_P	SATA1_TX_N		SATA1_RX_P	SATA1_RX_N	4
5	n.c.	n.c.		n.c.	n.c.	5
6	PCIE_PORT10_RX_P<1>	PCIE_PORT10_RX_M<1>		PCIE_PORT10_TX_P<1>	PCIE PORT10 TX M<1>	6
7	PCIE_PORT10_RX_P<3>	PCIE_PORT10_RX_M<3>		PCIE_PORT10_TX_P<3>	PCIE_PORT10_TX_M<3>	7
8	JTAG_TCK_RTM	JTAG_TMS_RTM		_88_RTM_SHIFT_CLK	_88_RTM_LATCH_CLK	8
9	Reserved	_88_RTM_PS0_N		_88_RTM_RST_KEY_N	_88_RTM_RST_OUT_N	9
10	n.c. (RTM_VP5)	RTM_ENABLE_N		_88_RTM_I2C_CLK	_88_RTM_I2C_DAT	10

Figure 3-24 P32 Backplane Connector Pinout - Rows A to D -



	a	b	ab	cd	ef	gh	c	d	
1	PCIE_PORT9_RX_P<0>	PCIE_PORT9_RX_M<0>					PCIE_PORT9_TX_P<0>	PCIE_PORT9_TX_M<0>	1
2	PCIE_PORT9_RX_P<2>	PCIE_PORT9_RX_M<2>					PCIE_PORT9_TX_P<2>	PCIE_PORT9_TX_M<2>	2
3	PCIE_PORT8_RX_P<0>	PCIE_PORT8_RX_M<0>					PCIE_PORT8_TX_P<0>	PCIE_PORT8_TX_M<0>	3
4	PCIE_PORT8_RX_P<2>	PCIE_PORT8_RX_M<2>					PCIE PORT8 TX P<2>	PCIE_PORT8_TX_M<2>	4
5	PCIE_PORT7_RX_P<0>	PCIE PORT7 RX M<0>					PCIE_PORT7_TX_P<0>	PCIE_PORT7_TX_M<0>	5
6	PCIE_PORT7_RX_P<2>	PCIE_PORT7_RX_M<2>					PCIE_PORT7_TX_P<2>	PCIE_PORT7_TX_M<2>	6
7	PCIE_PORT6_RX_P<0>	PCIE_PORT6_RX_M<0>					PCIE_PORT6_TX_P<0>	PCIE PORT6 TX M<0>	7
8	PCIE_PORT6_RX_P<2>	PCIE_PORT6_RX_M<2>					PCIE_PORT6_TX_P<2>	PCIE_PORT6_TX_M<2>	8
9	CLK100_RTMPCIE9_P	CLK100_RTMPCIE9_M					CLK100_RTMPCIE8_P	CLK100_RTMPCIE8_M	9
10	RTM_VP12	n.c (RTM_VP5)					n.c. (RTM_V3P3)	RTM_VP12	10

Figure 3-25 P32 Backplane Connector Pinout - Rows E to H -



	e	f	ab	cd	ef	gh	g	h	
1	PCIE_PORT9_RX_P<1>	PCIE_PORT9_RX_M<1>					PCIE_PORT9_TX_P<1>	PCIE_PORT9_TX_M<1>	1
2	PCIE_PORT9_RX_P<3>	PCIE_PORT9_RX_M<3>					PCIE PORT9 TX P<3>	PCIE_PORT9_TX_M<3>	2
3	PCIE_PORT8_RX_P<1>	PCIE_PORT8_RX_M<1>					PCIE_PORT8_TX_P<1>	PCIE_PORT8_TX_M<1>	3
4	PCIE_PORT8_RX_P<3>	PCIE_PORT8_RX_M<3>					PCIE_PORT8_TX_P<3>	PCIE_PORT8_TX_M<3>	4
5	PCIE_PORT7_RX_P<1>	PCIE PORT7 RX M<1>					PCIE_PORT7_TX_P<1>	PCIE_PORT7_TX_M<1>	5
6	PCIE_PORT7_RX_P<3>	PCIE_PORT7_RX_M<3>					PCIE_PORT7_TX_P<3>	PCIE_PORT7_TX_M<3>	6
7	PCIE_PORT6_RX_P<1>	PCIE_PORT6_RX_M<1>					PCIE_PORT6_TX_P<1>	PCIE_PORT6_TX_M<1>	7
8	PCIE_PORT6_RX_P<3>	PCIE_PORT6_RX_M<3>					PCIE PORT6 TX P<3>	PCIE_PORT6_TX_M<3>	8
9	CLK100 RTMPCIE7 P	CLK100_RTMPCIE7_M					CLK100_RTMPCIE6_P	CLK100 RTMPCIE6 M	9
10	n.c.	_88_RTM_PS0_N					_88_RTM_DI	_88_RTM_DO	10

4.1 Introduction

The Basic Input/Output System (BIOS) provides an interface between the operating system and the hardware of the blade. It is used for hardware configuration. Before loading the operating system, BIOS performs basic hardware tests and prepares the blade for the initial boot-up procedure.

During blade production, identical BIOS images are programmed into both boot flash banks. It is possible to select boot flash as device to boot from. This is done via an IPMI command. For further details refer to section *System Boot Options Commands* on page 225.

The BIOS used on the blade is based on the AMI UEFI BIOS with several Artesyn Embedded Technologies extensions integrated. Its main features are:

- Initialize CPU, chipset and memory
- Initialize PCI devices
- Setup utility for setting configuration data
- IPMC support
- Serial console redirection for remote blade access
- Boot operation system

The BIOS complies with the following specifications:

- UEFI Specification 2.0
- Plug and Play BIOS Specification 1.0A
- PCI BIOS Specification 2.1
- SMBIOS Specification 2.7
- BIOS Boot Specification 1.01
- Preboot Execution Environment (PXE) 2.1
- SMP 1.4
- Advanced Configuration and Power Interface (ACPI)3.0b

The BIOS setup program is required to configure the blade hardware. This configuration is necessary for operating the blade and connected peripherals. The configuration data are stored in the same flash device from which the board boots.

When you are not sure about configuration settings, restore the default values. This option is provided in case a value has been changed and you wish to reset settings. To restore the default values, press <F3> in Setup.

- Loading the BIOS default values will affect all setup items and will reset options previously altered.
- If you set the default values, the displayed default values takes effect only after the BIOS setup is saved and closed.

4.2 Accessing the Blade Using the Serial Console Redirection

The blade's firmware provides a serial console redirection feature allowing remote access to the blade through a terminal connected to the blade's serial interface.

The terminal can be connected to display VGA text information. Terminal keyboard input is redirected and treated as a normal PC keyboard input. The serial console redirection feature can be configured via a setup utility.

4.2.1 Requirements for Serial Console Redirection

For serial console redirection, the following is required:

- Terminal or terminal emulation which supports a VT100 mode
- NULL-modem cable

Terminal emulation programs such as TeraTermPro can be used. In order to use TeraTermPro using the function keys, the keyboard configuration file of TeraTermPro has to be modified as shown in the table below.

Table 4-1 BIOS Key Codes for Terminal Emulation Program

Function Key	Key Code
PF1	59
PF2	60

4.2.2 Default Access Parameters

By default, the blade can be accessed using the serial interface COM1. By default, this interface is accessible using a RJ-45 connector at the blade's faceplate.

A NULL-Modem cable is available as accessory kit for the blade. It converts the RJ-45 connector to a standard DSUB connector which can be connected to a remote terminal. The following communication parameters are used, by default:

- Baud rate: 9600
- Flow control: None
- VT-100
- 8 data bits
- No parity
- 1 stop bit

4.2.3 Connecting to the Blade

Procedure

To connect to the blade using the serial console redirect feature:

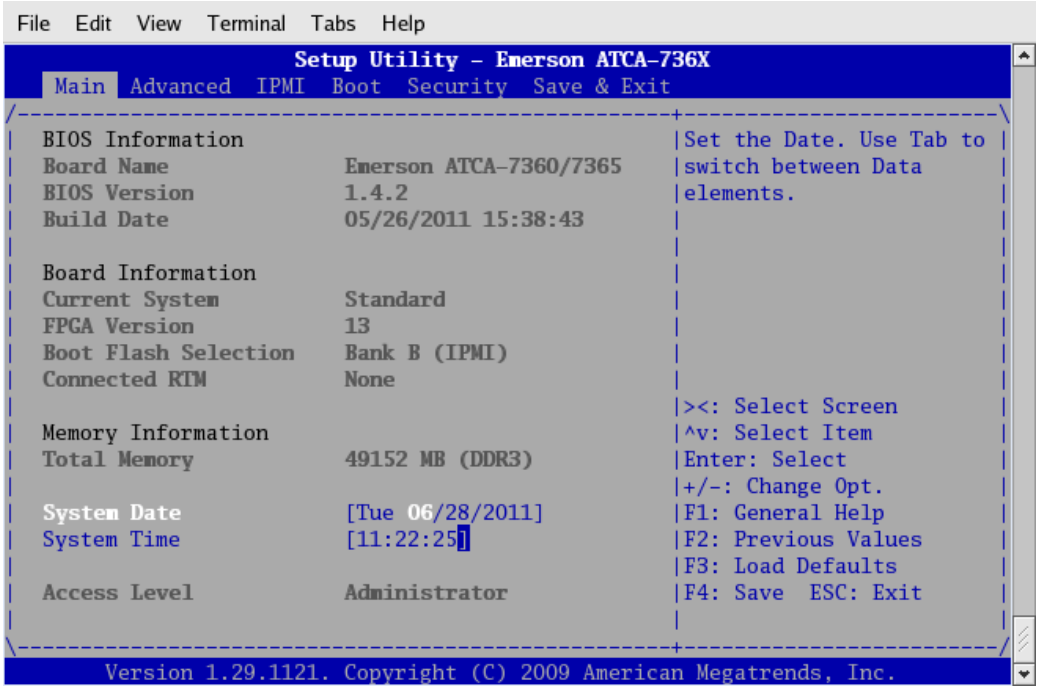
1. Configure terminal to communicate using the same parameters as in BIOS setup.
2. Connect terminal to NULL-modem cable.
3. Connect NULL-modem cable to COM port of the blade.
4. Start up blade.

4.3 Changing Configuration Settings

When the system is switched on or rebooted, the presence and functionality of the system components is tested by Power-On Self-Test (POST).

Press <F2> when requested. The main menu appears. It looks similar to the one shown in the following figure.

Figure 4-1 Main Menu



- Make sure that BIOS is properly configured prior to installing the operating system and its drivers.
- If you save changes in setup, the next time the blade boots up, BIOS will configure the system according to the setup selections stored. If those values cause the system boot to fail, reboot and enter setup to get the default values or to change the selections that caused the failure.

In order to navigate in setup, use the arrow keys on the keyboard to highlight items on the menu. All other navigation possibilities are shown at the bottom of the menu.

Additionally, an item-specific help is displayed on the right side of the menu window.

4.4 Boot Options

This section describes which boot devices are supported by the BIOS and how to select the boot device.

4.4.1 Supported Boot Devices

The BIOS supports booting from the following devices/sources:

- USB devices, such as floppy, CD ROM and hard disk
- Solid State Disk connected to the SATA interface. (available only when SSD SATA is assembled)
- Storage devices connected to the SAS controller (by RTM)
- Network (Front Panel Ethernet, Base Ethernet and Ethernet on RTM)
- Storage devices connected to the Fiber Channel module (by RTM)
- iSCSI block devices connected to Base or Fabric Ethernet

4.4.2 Selecting The Boot Device

There are two possibilities to determine the device from which BIOS attempts to boot:

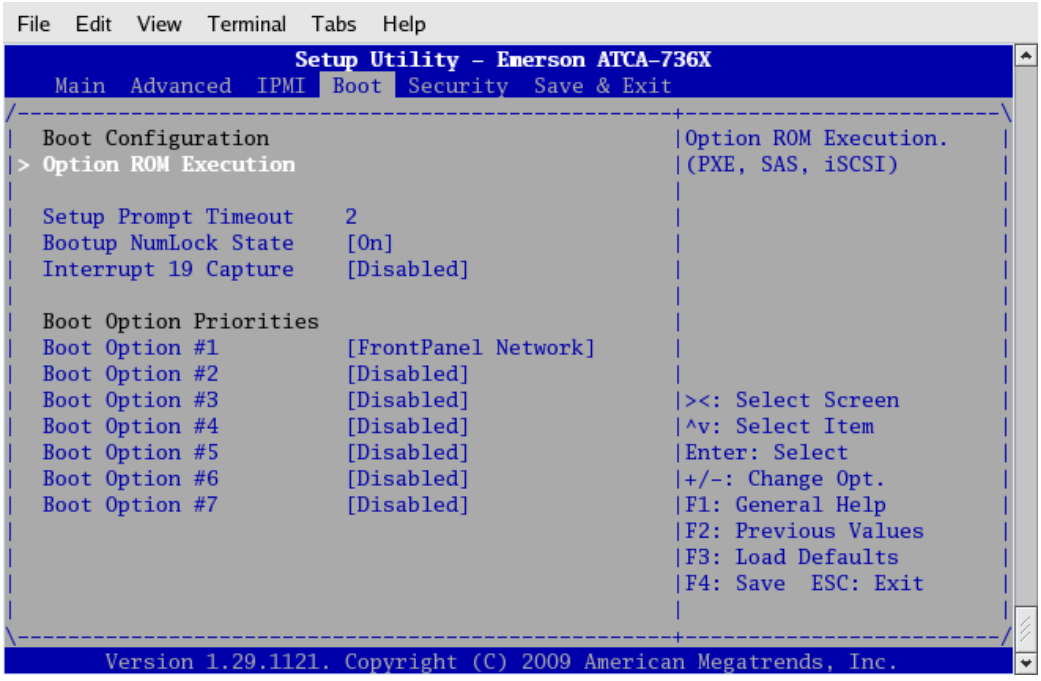
- By setup to select a permanent order of boot devices
- By boot selection menu to select any device for the next boot-up procedure only

By Setup

To select the boot device by setup, proceed as follows:

1. From the menu, select Boot.

Figure 4-2 Boot Menu



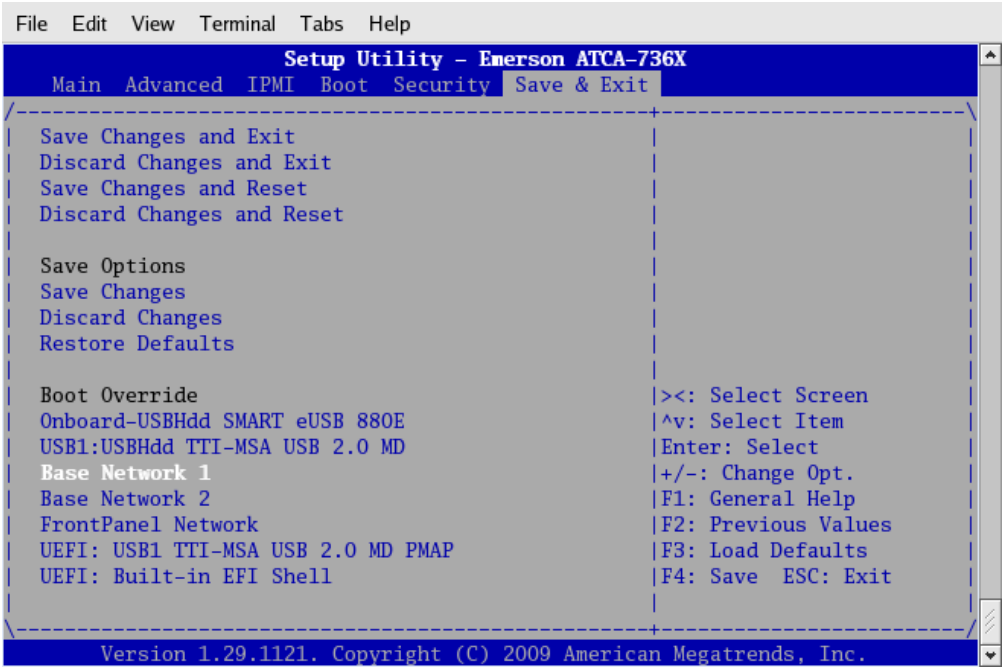
2. Select the order of the devices from which BIOS attempts to boot the operating system.
3. Enter the submenu "Option ROM Execution" to enable/disable booting from specific devices. Changes have to be saved and the board has to be rebooted when changing the Option ROM Execution.

If BIOS is not successful at booting from one device, it tries to boot from the next device on the list.

4.4.3 By Boot Selection Menu

1. From the menu, select Save & Exit.

Figure 4-3 Save and Exit Menu



2. Override existing boot sequence by selecting another boot device from the boot override list.

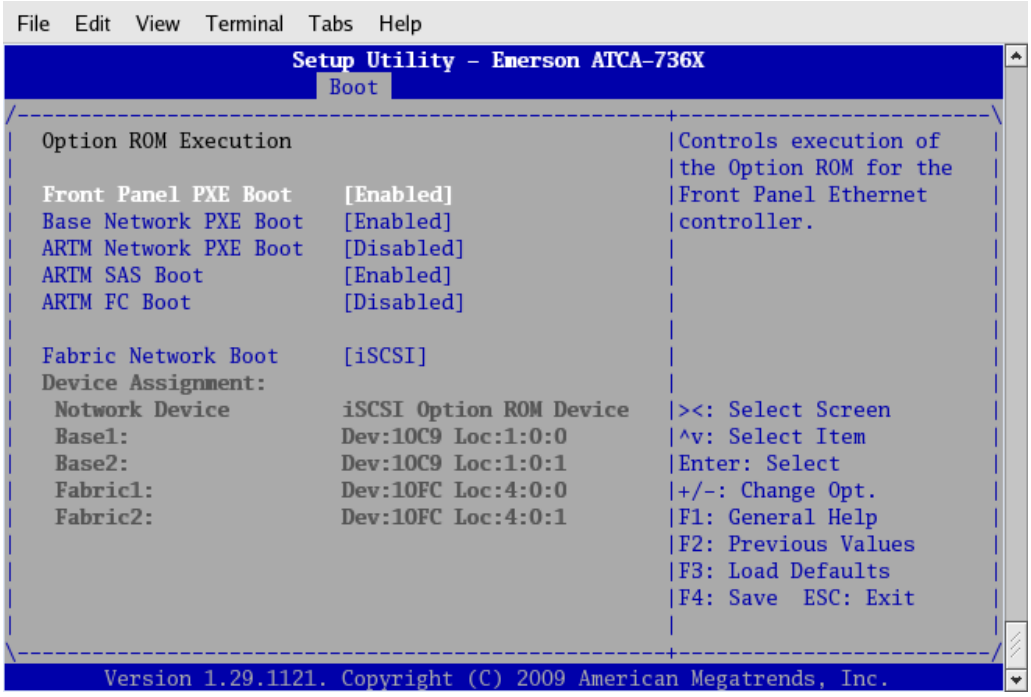
If the selected device does not load the operating system, BIOS resets the board and reverts to the previous boot sequence.

4.4.4 iSCSI Setup for Base and Fabric Ethernet

The board supports boot from iSCSI block devices connected to Base or Fabric Ethernet. To enable the iSCSI boot, proceed as follows:

1. From the menu, select Boot.
2. Under the Option ROM Execution sub menu, select the iSCSI item of Fabric Network Boot setup option.

Figure 4-4 Option ROM Execution

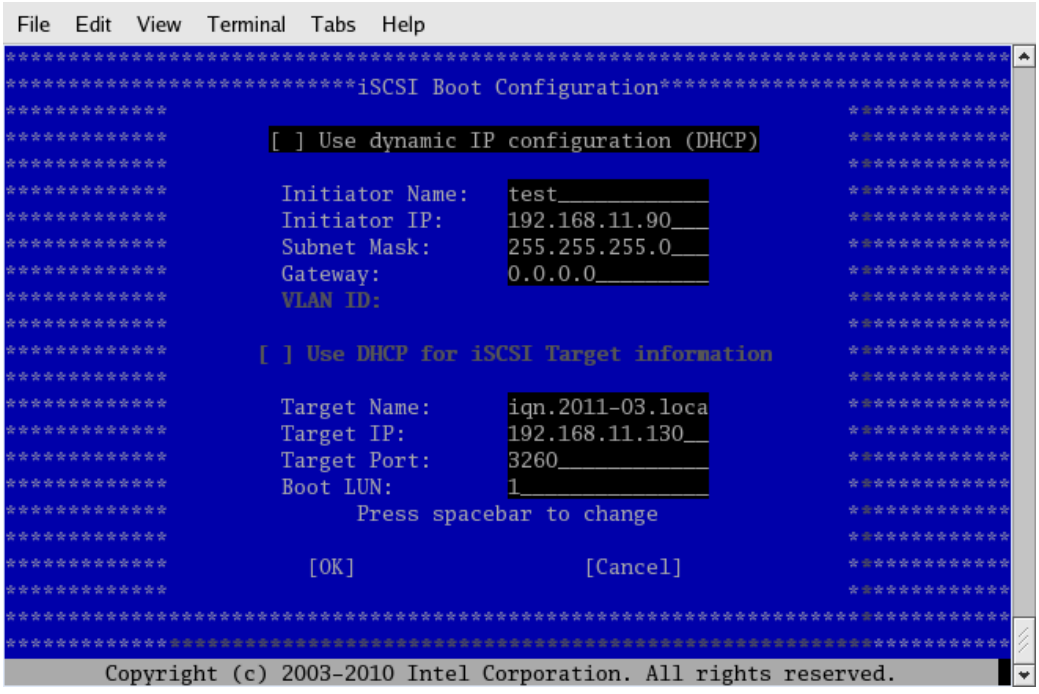


3. Save and Exit the BIOS setup.
4. To enter iSCSI setup, press Ctrl-D when the following message is displayed:
   "Intel(R) iSCSI Remote Boot version 2.7.53 Copyright (c) 2003-2010 Intel Corporation. All rights reserved. Press ESC key to skip iSCSI boot initialization. Press <Ctrl-D> to run setup.

4.4.4.1 iSCSI Boot Configuration

The following figure depicts the iSCSI Boot Configuration screen.

Figure 4-5 iSCSI Boot Configuration

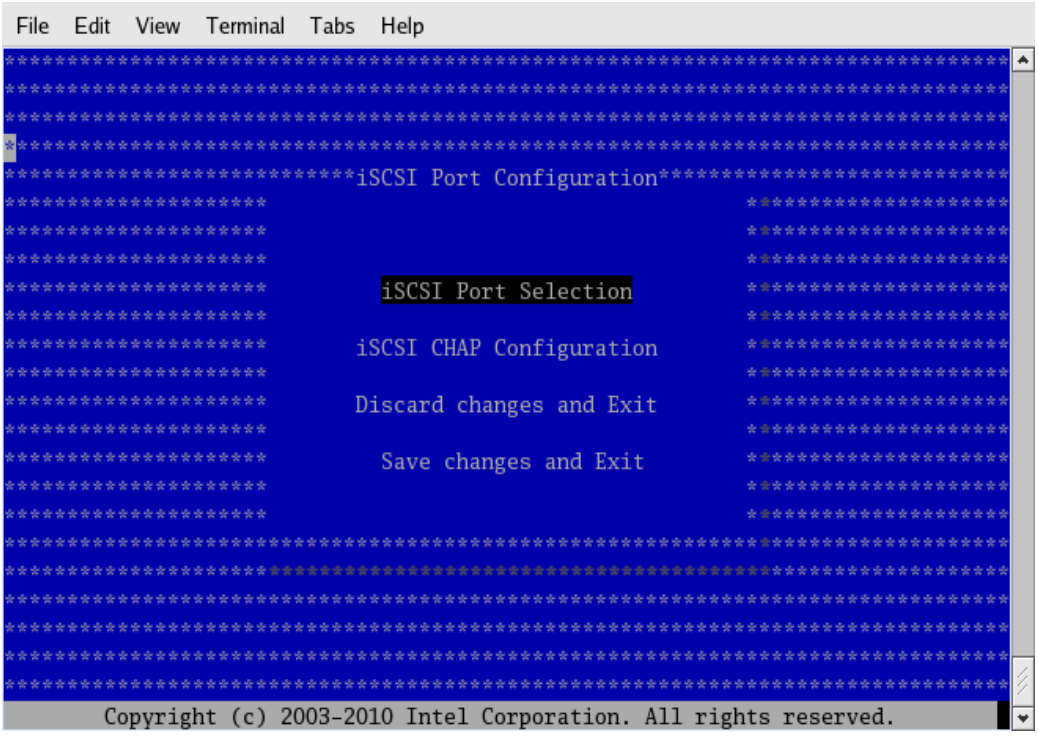


Enter Initiator and Target network configuration parameter

4.4.4.2 iSCSI Port Configuration

The following figure depicts the iSCSI Port Configuration screen.

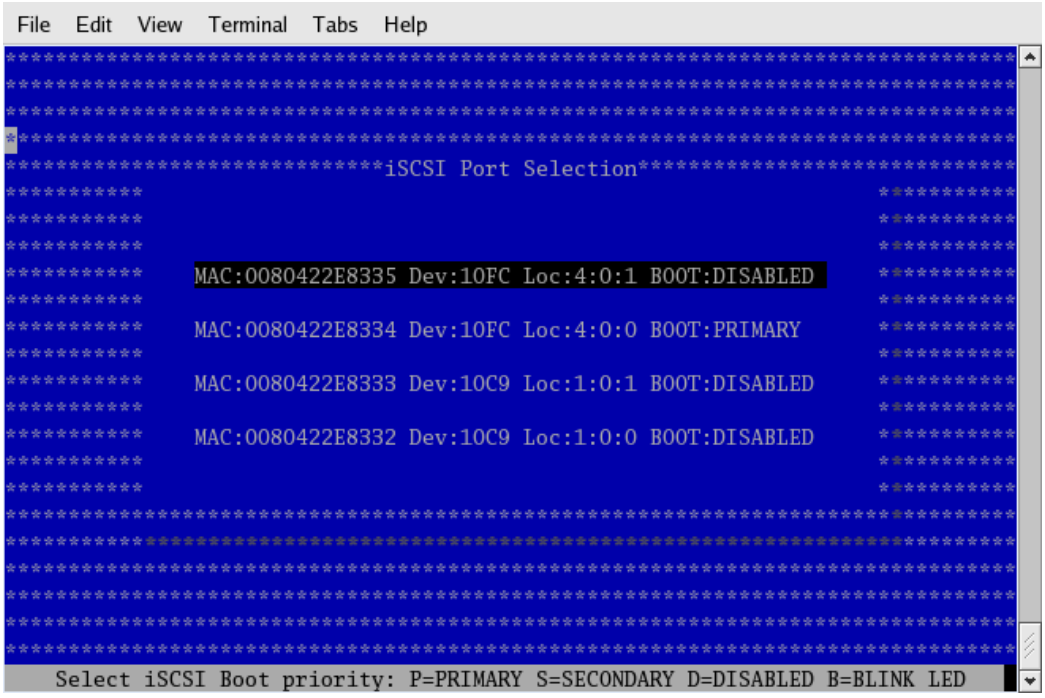
Figure 4-6 iSCSI Port Configuration



4.4.4.3 ISCSI Port Selection

The following figure depicts the iSCSI Port Selection screen.

Figure 4-7 iSCSI Port Selection



Enter Initiator and Target network configuration parameter.

The following table provides information about Ethernet Port Mapping.

Table 4-2 Ethernet port mapping

Network Device	iSCSI Option ROM Device
Base1	Dev:10C9 Loc:1:0:0
Base2	Dev:10C9 Loc:1:0:1
Fabric1	Dev:10FC Loc:4:0:0

Table 4-2 Ethernet port mapping (continued)

Network Device	iSCSI Option ROM Device
Fabric2	Dev:10FC Loc:4:0:1

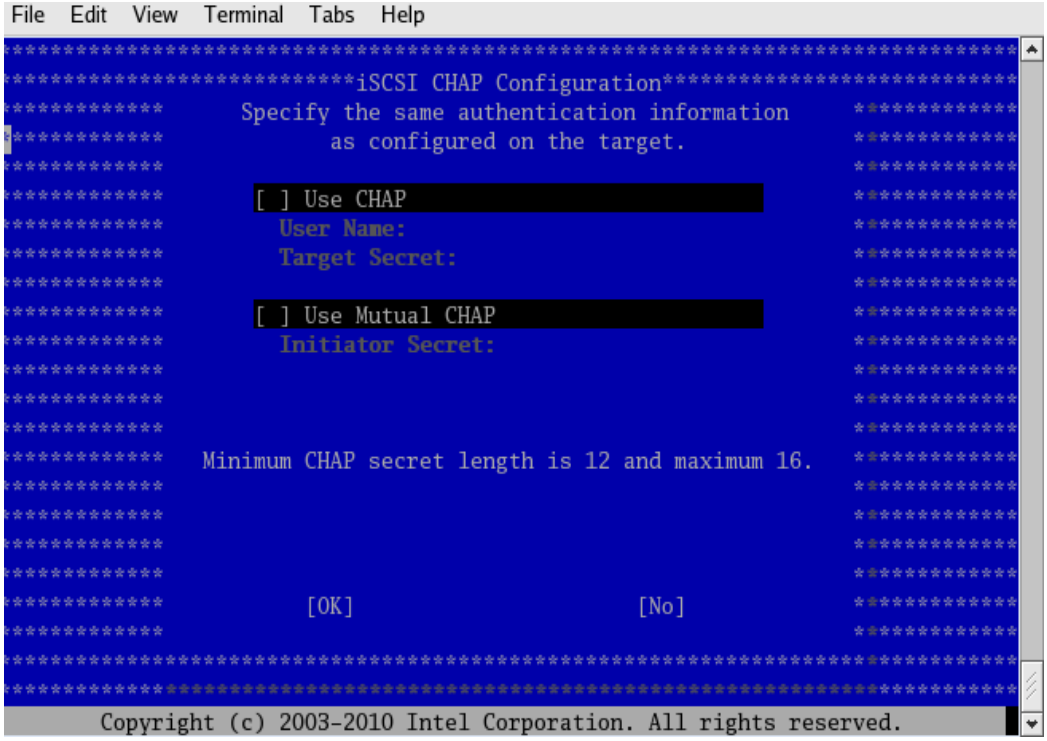
Table 4-3 Select iSCSI Boot priority hot keys

Key	Function
P	Selected device is primary boot device
S	Selected device is secondary boot device
D	Disable selected device
B	Blink LED (not supported)
Enter	Enter the Port configuration menu for the selected device

4.4.4.4 iSCSI Challenge Handshake Authentication Protocol (CHAP) Configuration

The following figure depicts the iSCSI CHAP Configuration screen.

Figure 4-8 iSCSI CHAP Configuration



Enter Challenge Handshake Authentication Protocol configuration parameter

4.5 BIOS Setup Configuration

4.5.1 Main

The following table contains description about the options that can be configured on Main

menu screen.

Table 4-4 Main Configuration

Item	Values	Description
System Date	[Thu 11/11/2010]	Set the Date. Use Tab to switch between Date elements
System Time	[15:48:21]	Set the Time. Use Tab to switch between Time elements

4.5.2 Advanced menu

4.5.2.1 Advanced -> CPU Configuration

The following table contains description about the options that can be configured in CPU Configuration.

Table 4-5 CPU Configuration

Item	Values	Description
Hyper-threading	Enabled (Default) Disabled	Enabled for OS optimized for Hyper-Threading Technology, Disabled for other OS not optimized for Hyper Threading Technology. When Disabled only one thread per enabled core is enabled.
Active Processor Core	All (Default) 1, 2, 3, 4, 5	Number of cores to enable in each processor package.
Limit CPUID Maximum	Enabled Disabled (Default)	If set to enabled, limits the CPUID instruction function 0 to return a maximum value of 3. Some operating systems like Windows NT cannot handle a value greater than 3. Default value is disabled. The CPUID instruction function 0 returns the number of the maximum standard functions.

Table 4-5 CPU Configuration (continued)

Item	Values	Description
Execute Disable Bit	Enabled (Default) Disabled	XD can prevent certain classes of malicious buffer overflow attacks when combined with a supporting OS e.g. Windows Server 2003 SP1, Windows Server 2008, Windows XP SP2, SuSE Linux 9.2 and newer, RedHat Enterprise 3 Update 3 and newer.)
Hardware Prefetcher	Enabled (Default) Disabled	To turn on/off the L2 Cache (MLC streamer) Prefetcher. See *CPU Performance Settings* on page 116
Adjacent Cache Line Prefetch	Enabled (Default) Disabled	To turn on/off prefetching of adjacent cache lines to L2 cache. See *CPU Performance Settings* on page 116.
L1 Data Prefetcher	Enabled (Default) Disabled	Enable/Disable L1 Data Prefetcher. See *CPU Performance Settings* on page 116
Data Reuse Optimization	Enabled (Default) Disabled	Data Reuse Performance Optimization for Server workloads. See *CPU Performance Settings* on page 116
Intel Virtualization	Enabled (Default) Disabled	When enabled, a VMM can utilize the additional hardware capabilities provided by Intel Virtualization Technology.
Turbo Mode	Enabled (Default) Disabled	Enable/Disable Turbo Mode. Turbo Mode allows processor cores to run faster than the marked frequency if the physical processor is operating below power, temperature and current specification limits.
Performance/Watt	Traditional (Default), Power Optimized	Optimized - Turbo Boost engages after highest performance state is sustained for more than 2 seconds. Traditional Intel Turbo Boost Technology is engaged immediately when possible.
CPU C3 Report	Enabled Disabled (Default)	Enable/Disable CPU C3 report to OS via ACPI table. CPU C3 state corresponds with ACPI C2 state. CPU C3: Execution Clock is stopped. Core Caches flushed. Intel recommends disabling CPU C3 report to OS.

Table 4-5 CPU Configuration (continued)

Item	Values	Description
CPU C6 report	Enabled (Default) Disabled	Enable/Disable CPU C6 report to OS via ACPI table. CPU C6 state corresponds with ACPI C3 state. CPU C6: Execution Clock stopped, Core states stored in the Last Level Cache, Core caches flushed. Intel recommends enabling CPU C6 report to OS.
Package C State limit	C0, C1, C3, C6, C7, No Limit (Default)	Specifies the lowest C-State (Low Power idle state) for the CPU package. Lower C states correspond lower power consumption and with a longer C-state entry/exit latency.
Socket 0 CPU Information		Show CPU 0 Information: CPU String, Stepping and Microcode Version
Socket 1 CPU Information		Show CPU 1 Information: CPU String, Stepping and Microcode Version

4.5.2.2 Advanced -> Memory Configuration

The following table contains description about the options that can be configured for Memory Configuration.

Table 4-6 Memory Configuration

Item	Values	Description
DIMM Information		Submenu for displaying DIMM presence and size information.
Memory Mode	Independent (Default), Mirroring, Lock-Step, Sparing	Select the mode for memory initialization See *Memory Configuration* on page 117
NUMA	Enable (Default) Disable	Enable/Disable support for Non uniform Memory Access (NUMA) aware Operating Systems. Select Enable for NUMA aware OS e.g Windows Server 2008. Linux with kernel 2.6.xx. Select Disable for all other. If enabled, BIOS creates the corresponding ACPI tables with Resource Affinity information. If disabled BIOS will set up memory interleaving between the two CPU packages.

Table 4-6 Memory Configuration (continued)

Item	Values	Description
Channel Interleaving	Auto (Default), 6 Way, 4 Way, 3 Way, 2 Way, 1 Way	Select different Channel Interleaving setting. Recommended value: Auto
RankInterleaving	Auto (Default), 4 Way, 2 Way, 1 Way	Select different rank Interleaving setting. Recommended value: Auto
Hardware Memory Test	Enable (Default) Disable	Enable/Disable hardware memory test.
Patrol Scrub	Enable (Default) Disable	Enable/Disable Patrol Scrubbing Feature. Patrol scrubs are intended to ensure that data with a correctable error does not remain in DRAM long enough to stand a significant chance of further corruption to an uncorrectable error. The Integrated Memory Controller will issue a Patrol Scrub in the background at a rate sufficient to write every line once a day.
Demand Scrub	Enable Disable (Default)	Enable/Disable Demand Scrubbing Feature. If a single ECC memory error is detected during normal read/write operation, the correct data and ECC check bits will be written back to memory.

4.5.2.3 Advanced -> Chipset - North Bridge

The following table contains description about the options that can be configured for Chipset-North Bridge.

Table 4-7 Chipset - North Bridge

Item	Values	Description
Auto-Detect RTM	Enable (Default) Disable	If enabled, the RTM is detected and the RTM PCIe parameter are set for this RTM. If disabled the RTM PCIe parameter can be set manually.
RTM PCIe Gen1 Speed	Enable Disable	This option force RTM PCIe root ports to Gen1 operation. If this option is disabled RTM PCIe support both Gen1 and Gen2 devices. This option is active when Auto-Detect RTM is set to Enable.

Table 4-7 Chipset - North Bridge (continued)

Item	Values	Description
PCIe to RTM	x4x4x4x4, x4x4x8, x8x4x4, x8x8, x16	Selects PCIe port Bifurcation for Zone 3 connector (RTM). This option is active when Auto-Detect RTM is set to Enable.

4.5.2.3.1 Advanced -> Chipset - North Bridge -> Intel(R) VT for Directed I/O Configuration

The following table contains description about the options that can be configured for Intel (R) VT for Directed I/O Configuration.

Table 4-8 Chipset - North Bridge -> Intel(R) VT for Directed I/O Configuration

Item	Values	Description
Intel(R) VT-d	Enable Disable (Default)	Enable/Disable Intel® Virtualization Technology for Directed I/O. VT-d extends Virtualization Technology by providing hardware support for I/O-device virtualization.
Interrupt Remapping	Enable (Default) Disable	Enable/Disable VT-d Engine Interrupt Remapping support.
Coherency Support	Enable Disable (Default)	Enable/Disable VT-d Engine Coherency support
ATS Support	Enable Disable (Default)	Enable/Disable VT-d Engine Address Translation Services (ATS) support.
Pass-through DMA	Enable (Default) Disable	Enable/Disable VT-d Engine Pass through DMA support.

4.5.2.3.2 Advanced -> Chipset - North Bridge -> IOH Thermal Sensors

The following table contains description about the options that can be configured for IOH Thermal Sensors.

Table 4-9 **Chipset - North Bridge -> IOH Thermal Sensors**

Item	Values	Description
Thermal Sensors	Enable Disable (Default)	Enables/disables integrated North Bridge thermal sensors. Recommended value: Disable
Low Threshold	70..127 Default 90	Low temperature threshold for thermal sensor.
High Threshold	70..127 Default 100	High temperature threshold for thermal sensor.
Catastrophic Threshold	70..127 Default 110	Critical temperature threshold for thermal sensor.

4.5.2.4 Advanced -> Chipset - South Bridge

The following table contains description about the options that can be configured for Chipset-South Bridge.

Table 4-10 Chipset - South Bridge

Item	Values	Description
Front Panel Ethernet	Enable (Default) Disable	Enable/Disable Front Panel Ethernet Controller
High Precision Timer	Enable (Default) Disable	Enable/Disable the High Precision Event Timer

4.5.2.4.1 Advanced -> Chipset - South Bridge -> USB Configuration

The following table contains description about the options that can be configured for USB Configuration under Chipset - South Bridge.

Table 4-11 Chipset - South Bridge -> USB Configuration

Item	Values	Description
All USB Devices	Enabled (Default) Disabled	Enable/Disable All USB devices.

Table 4-11 Chipset - South Bridge -> USB Configuration (continued)

Item	Values	Description
USB 2.0(EHCI) Support	Enabled (Default) Disabled	Enable/Disable USB 2.0 (EHCI) Support
Front Panel USB	Enabled (Default) Disabled	Enable/Disable Front Panel USB
Onboard USB Flash Disk	Enabled (Default) Disabled	Enable/Disable Onboard USB FlashDisk
ARTM USB	Enabled (Default) Disabled	Enable/Disable USB on ARTM

4.5.2.5 Advanced -> SATA Configuration

The following table contains description about the options that can be configured for SATA Configuration.

Table 4-12 Advanced -> SATA Configuration

Item	Values	Description
SATA Mode	Disable, IDE Mode (Default), AHCI Mode, RAID Mode	Select the SATA Mode: Disable: Disable the SATA controller IDE Mode: SATA controller works in IDE compatible mode. AHCI Mode: STATA controller works in AHCI Mode RAID Mode: STATA controller works in RAID Mode, Additionally a SATA RAID Option Rom is loaded.
SATA Controller 0	Disable, Enhanced, Compatible (Default)	Disable or select mode of Serial ATA Controller 0. Enhanced: work in SATA mode Compatible: work in IDE compatible mode. Only available when SATA Mode is set to IDE mode.
SATA Controller 1	Disable, Enhanced (Default)	Disable or select mode of Serial ATA Controller 1. Enhanced: work in SATA mode Only available when SATA Mode is set to IDE mode.

4.5.2.6 Advanced -> USB Configuration

The following table contains description about the options that can be configured for USB Configuration.

Table 4-13 Advanced -> USB Configuration

Item	Values	Description
Legacy USB Support	Enabled (Default) Disabled	Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.
EHCI Hand-off	Enabled (Default) Disabled	Select Disabled to enable a workaround for OS without EHCI hand-off support.
Port 60/64 Emulation	Enabled (Default) Disabled	Enables I/O port 60h/64h emulation support. This should be enabled for the complete USB keyboard legacy support for non-USB aware OS.
Device Reset timeout	10..40 seconds Default 20 sec.	USB mass storage device Start Unit command timeout. 10, 20, 30, 40 seconds.
Controller Timeout	1..20 seconds Default 20 sec.	The time out value for Control, bulk & interrupt transfer. 1, 5, 10, 20 seconds.
USB Device Name	Auto, Floppy, Forced FDD, Hard Disk, CD-ROM	Mass storage device emulation type. 'AUTO' enumerates devices according to their media format. Devices less than 530MB are detected as floppies. Optical drives are emulated as 'CD-ROM', drives with no media will be emulated according to a drive type. Forced FDD option can be used to force HDD formatted drive to boot as FDD (for example, ZIP drive).

4.5.2.7 Advanced -> Super IO Configuration

4.5.2.7.1 Advanced -> Super IO Configuration -> Serial Port 0 Configuration

The following table contains description about the options that can be configured for Serial Port 0 Configuration.

Table 4-14 Super IO Configuration -> Serial Port 0 Configuration

Item	Values	Description
Serial Port	Enabled (Default) Disabled	Enable or Disable Serial Port (COM 0)
ChangeSettings	Auto, IO=3F8h IRQ=4 (Default), IO=3F8h IRQ=3,4,5,6,7,10,11,12, IO=2F8h IRQ=3,4,5,6,7,10,11,12, IO=3E8h IRQ=3,4,5,6,7,10,11,12, IO=2E8h IRQ=3,4,5,6,7,10,11,12	Select IO port and Interrupt settings for COM 0

4.5.2.8 Advanced -> Serial Port Console Redirection

The following table contains description about the options that can be configured for Serial Port Console Redirection.

Table 4-15 Advanced -> Serial Port Console Redirection

Item	Values	Description
Console Redirection	Enabled (Default) Disabled	Enable/Disable Console Redirection
Console Redirection	Enabled (Default) Disabled	Enable/Disable Console Redirection for Windows Emergency Management Services (EMS)
Terminal Type	VT100, VT100+, VT-UTF8 (Default), ANSI	VT-UTF8 is the preferred terminal type for out-of-band Windows EMS management. The next best choice is VT100+ and then VT100.

4.5.2.8.1 Advanced -> Serial Port Console Redirection -> Console Redirection Settings

The following table contains description about the options that can be configured for Console Redirection Settings.

Table 4-16 Serial Port Console Redirection -> Console Redirection Settings

Item	Values	Description
Terminal Type	VT100 (Default), VT100+, VT-UTF8, ANSI	Terminal Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
Bits per second	9600 (Default), 19200, 57600, 115200	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
Data Bits	7, 8 (Default)	Data Bits
Parity	None (Default), Even, Odd, Mark, Space	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the number of 1's in the data bits is even. Odd: parity bit is 0 if number of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection.
Stop Bits	1 (Default), 2	Stop bits indicate the end of a serial data packet. The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.
Recorder Mode	Enabled, Disabled (Default)	On this mode enabled only text will be send. This is to capture Terminal data.
Resolution100x31	Enabled, Disabled (Default)	Enables or disables extended terminal resolution.
Legacy OS Redirection	80x24 (Default), 80x25	Specifies the Number of Rows and Columns supported by legacy serial redirection.

4.5.2.9 Advanced -> UEFI Network Stack

The following table contains description about the options that can be configured for UEFI Network Stack.

Table 4-17 Advanced -> UEFI Network Stack

Item	Values	Description
UEFINetworkstack	Enable, Disable (Default)	Enable/Disable the UEFI network stack. This is needed for UEFI network boot (PXE and iSCSI).

4.5.2.10 Advanced -> Runtime Error Logging

The following table contains description about the options that can be configured for Runtime Error Logging.

Also, refer *Runtime Error Logging* on page 121.

Table 4-18 Advanced -> Runtime Error Logging

Item	Values	Description
Runtime Error Logging	Enabled (Default) Disabled	Enable/Disable Runtime Error Logging Support. Events are sent to SMBIOS error log and IPMI SEL.
PCI Error Logging	Enabled (Default) Disabled	Enable/Disable PCI Error Logging.
Error Threshold	1...1000, Default 10	Memory Correctable Error Threshold value. Range [1..1000] Default 10.
Error Logging Limit	1...20 Default 10	Memory Correctable Error Logging Limit value. Range [1..20] Default 10.

4.5.2.11 Advanced -> SMBIOS Event Log

4.5.2.11.1 Advanced -> SMBIOS Event Log -> SMBIOS Event Log Settings

The following table contains description about the options that can be configured for MBIOS Event Log Settings.

See also *SMBIOS Error Logging* on page 125

Table 4-19 SMBIOS Event Log -> SMBIOS Event Log Settings

Item	Values	Description
SMBIOS Event Log	Enabled (Default) Disabled	Change this to enable or disable all features of SMBIOS Event Logging during boot.
Erase Event Log	No (Default), Yes On next reset, Yes On every reset	Choose options for erasing SMBIOS Event Log. Erasing is done prior to any logging activation during reset.
When Log is Full	Do Nothing (Default), Erase Immediately	Choose options for reactions to a full SMBIOS Event Log. This option does not take effect until the computer is restarted.
Log EFI OEM Errors	Enabled (Default) Disabled	Enable or disable the logging of EFI Error Codes as OEM Codes.
Convert OEM Codes	Enabled (Default) Disabled	Enable or disable the converting of EFI Error Codes to Standard SMBIOS Types. EFI Errors which cannot be translated are logged as SMBIOS Post Errors.
Inject Errors	Enabled Disabled (Default)	Inject Errors before booting a OS: Following errors are injected: No Console found, IPMI Boot Parameter Checksum error, CPU Self test failure, Bad Battery.

4.5.2.12 Advanced -> Local IPMI System Event Log

The following table contains description about the options that can be configured for Local IPMI System Event Log.

Table 4-20 Advanced -> Local IPMI System Event Log

Item	Values	Description
Erase Local SEL	No (Default), Yes On next reset, Yes On every reset	Choose options for erasing local SEL. This option does not take effect until the computer is restarted.

4.5.2.13 Advanced -> WHEA Configuration

The following table contains description about the options that can be configured for Serial Port Console Redirection.

Table 4-21 Advanced -> WHEA Configuration

Item	Values	Description
WHEA Support	Enable, Disable (Default)	Enable or disable support for Windows Hardware Error Architecture.

4.5.3 IPMI

4.5.3.1 IPMI -> IPMI Watchdog Configuration

The following table contains information about the options available for IPMI Watchdog Configuration.

Table 4-22 IPMI -> IPMI Watchdog Configuration

Item	Values	Description
POST Timer (FRB2)	Enable, Disable (Default)	Enable or Disable FRB2 timer (POST timer). This watchdog monitors BIOS initialization tasks.
FRB2 Timer timeout	3, 4, 5, 6 minutes Default 6 minutes	Enter value Between 3 to 6 min for FRB2 Timer Expiration value. Not available if Frb2 Timer is disabled.
FRB2 Timeout Action	Do Nothing, Reset (Default), Power Down Power Cycle	Configure how the system should respond if the Frb2 Timer expires. Not available if Frb2 Timer is disabled.
O/S Watchdog Timer	Enable, Disable (Default)	If enabled, starts a BIOS timer just before booting the OS. The OS has to shut off the watchdog timer when successfully booted.
O/S Watchdog Timer Timeout	1,2,3,5, 7, 10, 15, 20 minutes Default 5 minutes	Configure the time out of the O/S Boot Watchdog Timer. Not available if O/S Boot is disabled.

Table 4-22 IPMI -> IPMI Watchdog Configuration (continued)

Item	Values	Description
O/S Watchdog Timeout Action	Do Nothing, Reset (Default), Power Down	Configure how the system should respond if the O/S Boot Watchdog Timer expires. Not available if O/S Boot Watchdog Timer is disabled.

4.5.3.2 IPMI -> System Event Log

The following table contains information about the options available for System Event Log.

Table 4-23 IPMI -> System Event Log

Item	Values	Description
Log EFI Status Codes	Disabled, Both (Default), Error code, Progress code	Configure the logging of EFI Status Codes to IPMI Firmware Progress/Error events and other Status/Error IPMI events. See chapter 4.10.3 IPMI Error Logging

4.5.4 iSCSI

This menu is for configuration of iSCSI boot of UEFI compatible Operating Systems. iSCSI boot is enabled when UEFI Network stack is set to Enabled (see BIOS setup Advanced -> UEFI Network Stack link).

For every network device, there is a submenu for configuration of iSCSI boot.

Table 4-24 iSCSI

Item	Values	Description
iSCSI Initiator Name		The worldwide unique name of the initiator. Only IQN (iSCSI Qualified Name) format is accepted.
Enable iSCSI	Enable, Disable (Default)	Enable/Disable iSCSI for this Ethernet Port.
Enable DHCP	Enable, Disable (Default)	Enable/Disable DHCP to retrieve IP address, Subnet Mask, Gateway.
Initiator IP Address	0.0.0.0	IP Address of the Initiator. Not available when DHCP is enabled.

Table 4-24 iSCSI (continued)

Item	Values	Description
Initiator Subnet Mask	0.0.0.0	Subnet Mask for the Initiator Network. Not available when DHCP is enabled.
GateWay		Enter IP Address of Gateway. Not available when DHCP is enabled.
Get target info via DHCP	Enable, Disable (Default)	Get target info via DHCP.
Target Name		Enter the Target Name. Not available when DHCP is enabled.
Target IP Address	0.0.0.0	IP Address of the Target. Not available when DHCP is enabled.
Target Port	0	Target Port. Not available when DHCP is enabled.
Boot LUN	0	Hexadecimal representation of the LUNumber. Examples are, 4752-3A4F-6b7e-2F99, 6734-9-156f-127, 4186-9. Not available when DHCP is enabled.
CHAP Type	None (Default), One Way, Mutual	Select the CHAP (Challenge-Handshake Authentication Protocol) type.
Save Changes		Press Enter to Save Changes
Back To Previous Page		Press Enter to Return to the previous Page (same as ESC)

4.5.5 Boot

The following table contains information about the options available on Boot menu screen.

Table 4-25 Boot

Item	Values	Description
Setup Prompt Timeout	0..65535 seconds Default 2 seconds	Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.
Bootup NumLock State	On/off Default on	Select the keyboard NumLock state.

Table 4-25 Boot (continued)

Item	Values	Description
Interrupt 19 Capture	Enable, Disable (Default)	If enabled, allows Option ROMs to trap Int 19. This is needed for some SCSI/SAS controller.
Boot Option Priorities		Select the boot device order.

4.5.5.1 Boot -> Option ROM Execution

The following table contains information about the options available for Option ROM Execution.

Table 4-26 Boot -> Option ROM Execution

Item	Values	Description
Front Panel Net Boot	Enabled (Default), Disabled	Controls execution of the Option ROM for the Front Panel Ethernet controller. Select Enabled when Front Panel Boot is required.
Base Network Boot	Enabled (Default), Disabled	Controls execution of the Option ROM for both Base Network Ethernet controller. Select Enabled when Base Network Boot is required.
Fabric Network Boot	Enabled (Default), Disabled	Controls execution of the Option ROM for both Fabric Network Ethernet controller. Select Enabled when Fabric Network Boot is required.
ARTM Network Boot	Enabled, Disabled (Default)	Controls execution of the Option ROM for RTM Network Ethernet controller. Select Enabled when RTM Network Boot is required.
ARTM SAS Boot	Enabled (Default), Disabled	Controls execution of the Option ROM for RTM SAS controller. Select Enabled when RTM SAS Boot is required.
ARTM FC Boot	Enabled, Disabled (Default)	Controls execution of the Option ROM for RTM Fibre Channel controller. Select Enabled when RTM Fibre Channel Boot is required.

4.5.6 Security

If ONLY the Administrator's password is set, then this only limits access to Setup and is only asked for when entering Setup If ONLY the User's password is set, then this is a power on password and must be entered to boot or enter Setup. In Setup the User will have Administrator rights.

4.5.7 Save & Exit

The following table contains information about the options available on Save & Exit screen.

Table 4-27 Save & Exit

Item	Description
Save Changes and Exit	Exit BIOS setup after saving the changes.
Discard Changes and Exit	Exit BIOS setup without saving any changes.
Save Changes and Reset	Reset the system after saving the changes.
Discard Changes and Reset	Reset system setup without saving any changes.
Save Changes	Save Changes done so far to any of the setup options.
Discard Changes	Discard Changes done so far to any of the setup options.
Restore Defaults	Restore/Load Defaults values for all the setup options.
Boot Override	Select a Boot Device to boot one time. Boot order is not changed.

4.6 CPU Performance Settings

In order to get optimal performance, Intel recommends different settings of the CPU prefetcher for Westmere EP (Xeon 56xx) CPUs.

See *Advanced -> CPU Configuration* on page 100.

Depending on the main purpose of the blade, the following settings are recommended:

- HPC and General Purpose Server:

```
Hardware Prefetcher          [Enabled]
Adjacent Cache Line Prefetch [Enabled]
L1 Data Prefetcher           [Enabled]
DataReuse Optimization       [Enabled]
```

- Enterprise Platforms:

```
Hardware Prefetcher          [Disabled]
Adjacent Cache Line Prefetch [Disabled]
L1 Data Prefetcher           [Disabled]
DataReuse Optimization       [Disabled]
```

It is recommended to test the application which will run on the blade with different CPU settings in order to select the best configuration.

4.7 Memory Configuration

The Intel Xeon processor 5600 series supports four different memory RAS (Reliability, Availability, and Serviceability) Modes: Independent Channel Mode, Spare Channel Mode, Mirrored Channel Mode, and Lockstep Channel Mode.

4.7.1 Independent Channel Mode

In independent mode, all three channels are operating independently. The ECC code appears in each independent channel. Failure of the DRAM can be corrected. The correction capabilities in independent mode are:

- Correction of any x4 DRAM device failure.
- Detection of 99.986% of all single bit failures that occur in addition to an x4 DRAM failure.
- Detection of any 2-bit uncorrectable errors.

4.7.2 Spare Channel Mode

In Spare Channel Mode, Channel 0 and 1 are active channels and Channel 2 is the spare of the other two channels. The spare channel is held in reserve and is not available as system memory. The spare channel must have identical population to the channel being copied from. This means that all three channels must have identical population with regards to size and organization. DIMM slot populations. The Memory Controller will maintain correctable ECC error counters for each DIMM in the system that can either trigger an SMI event or be periodically polled by software to determine whether a high error rate is happening. SMI Software can then configure the Integrated Memory Controller to copy contents from one channel to another.

4.7.3 Mirrored Channel Mode

The Integrated Memory Controller supports mirroring across channels. DIMM organization in each slot of one channel must be identical to the DIMM in the corresponding slot of the other channel. When mirroring is enabled, the memory image in Channel 0 is maintained the same as Channel 1. DIMMs in Channel 2 are unused.

Uncorrectable errors are logged and signaled as correctable, but change the channel state to "Disabled", and the working partner to Redundancy Loss.

4.7.4 Lockstep Channel Mode

The Lockstep configuration requires a minimum of two DIMMs one in Channel 0 and Channel 1. Channel 2 is not used in Lockstep Channel Mode. The ECC DRAM on each DIMM is mapped to two adjacent symbols, so any failure of the DRAM can be corrected. The correction capabilities in lockstep mode are:

- Correction of any x4 or x8 DRAM device failure.
- Detection of 99.986% of all single bit failures that occur in addition to an x8 DRAM failure. The Memory Controller will detect a series of failures on a specific DRAM and use this information in addition to the information provided by the code to achieve 100% detection of these cases.
- Detection of all permutations of 2 x4 DRAM failures.

4.8 Restoring BIOS Default Settings

The blade provides an on-board configuration switch that allows to load BIOS settings from the DEFAULT area of the IPMI Boot Parameters. In order to restore the BIOS default settings using this switch, you have to proceed as follows.

Procedure

To restore the BIOS default settings, proceed as follows:

1. Remove the blade from the system.
   See *Installing and Removing the Blade* on page 59 for the exact procedure.
2. Set the on-board switch SW4-3 OFF and SW4-4 ON.
   See *Switch Settings* on page 52 for the exact location of SW4.
3. Install and power up the blade.
   See *Installing and Removing the Blade* on page 59 for the exact procedure.
4. Wait until the blade has completely booted and is up and running.
5. Remove the blade from the system again.
   See *Installing and Removing the Blade* on page 59 for the exact procedure.
6. Set switch SW4-3 and SW4-4 to OFF.
   Now the BIOS default settings are restored.

4.9 Shelf Slot Power Requirement

The ATCA-7365-CE always requests from the shelf manager to run at full performance (300 Watt). The system needs to support this for the slot used for the ATCA-7365-CE so that the shelf manager will enable the board at that power level.

In older systems supporting only slots with 200 Watts, the shelf manager may not grant the power level requested and may not enable the board.

4.10 LED Usage

BIOS uses LEDs U1, U2 and U3 on the front panel to indicate activity of start up progress.

In boot loader phase (PEI phase) U1 and U2 glow red, U3 is glowing alternately red, green and orange.

In main initialization phase (DXE phase) only U3 is glowing alternately red, green and orange. U1 and U2 are set to the default value: base Ethernet interface link and activity LEDs.

Shortly before closing BIOS and starting an operation system, LED U3 is set to OFF.

4.11 Upgrading the BIOS

A BIOS upgrade kit for the blade is available. This allows the BIOS to be upgraded. The BIOS upgrade kit contains documentation which describes in detail how to upgrade the BIOS.

Update tool for Linux is provided with Basic Blade Services (BBS). For details on how to upgrade BIOS from Linux, please refer to *Basic Blade Services Software for the ATCA-7365 Programmer's Reference*.

The BIOS can also be upgraded via IPMI - HPM.1 (Hardware Platform Management IPM Controller Firmware Upgrade). Please refer to *Firmware Upgrade* on page 277.

After performing a BIOS upgrade or after restoring a corrupted BIOS image, all BIOS settings are reset to their default values except for parameters that are stored in IPMC storage area. See Table "System Boot Options Parameter #100 - Supported Parameters" on page 232.

4.12 BIOS Error Logging

BIOS supports the following methods to report errors:

- SMBIOS error logging
- IPMI event logging
- Error logging to the console

4.12.1 Runtime Error Logging

BIOS supports Runtime Error Logging for memory errors and PCI errors. See BIOS Setup Advanced -> Runtime Error Logging. Errors are logged to the IPMI controller and to the SMBIOS event log.

The Runtime Error Logging can be enabled or disabled. If enabled, the PCI Error Logging can be enabled or disabled separately.

For correctable memory error logging, there are two additional parameters to prevent the flooding of the event logs. The parameters are:

- Error Threshold - Correctable memory errors are logged when the threshold is reached. The first correctable memory error is always logged.
- Error Logging Limit - The number of logged correctable memory errors for a DIMM is limited. If the last entry in the log is SMBIOS: 'Correctable memory log disabled' and IPMI: Memory event 'Correctable ECC logging limit reached'. No further correctable errors are logged for this DIMM.

Table 4-28 Logged Error Events

Error	SMIBIOS	IPMI
Correctable: - Correctable ECC Memory Error	Single-bit ECC memory error	Sensor: Memory, Offset 00h
Correctable: - Memory Error Limit Reached - Correctable ECC logging limit reached	Correctable memory log disabled	Sensor: Memory, Offset 05h
Uncorrectable: - Uncorrectable ECC Memory Error	Multi-bit ECC memory error	Sensor: Memory, Offset 01h
PCI PERR	PCI Parity Error	Sensor: Critical Interrupt, Offset 04h PCI PERR
PCI SERR	PCI System Error	Sensor: Critical Interrupt, Offset 05h PCI SERR

4.12.2 Error Simulation

For test purposes, it is possible to inject errors.
Enable 'Inject Errors' in 'Event Logs' -> 'SMBIOS Event Log Settings' in BIOS setup.

The following errors are injected short before the OS is booted:

- No Console found
- IPMI Boot Parameter Checksum error
- CPU Self test failure
- Bad battery

These errors are logged to SMBIOS error log, IPMI error log (local SEL and Shelf manager) and to the console.

4.12.3 IPMI Error Logging

BIOS generates status events like Firmware Progress event and error events.
The table below shows all BIOS supported IPMI Sensors and their possible events.

Table 4-29 BIOS Supported IPMI Events

Sensor	Event
System Firmware Progress (0Fh)	Offset 00h System Firmware Error Supported Event Data2: 00h unspecified Error 01h No system memory 02h No usable system memory 03h SATA device failure 07h No console in found 0Ah No console out found 0Bh Firmware ROM corrupted FDh OEM Error Extension Supported Event Data3 09h Flash Write Error 21h CPU BIST Error 22h PCI Out Of Resource 50h IPMI Boot Parameter Default Area Read Error 51h IPMI Boot Parameter Default Area Locked 52h IPMI Boot Parameter Default Area Checksum Error 53h IPMI Boot Parameter User Area Read Error 54h IPMI Boot Parameter User Area Locked 55h IPMI Boot Parameter User Area Checksum Error 56h IPMI Boot Parameter User Area Write Error 60h North Bridge Error 62h No Space for Legacy OptionROM Offset 02h System Firmware Progress Supported Event Data2: 01h Memory initialization 02h Hard-Disk (SATA) initialization 03h Secondary processor initialization 04h User authentication 05h User-initiated system setup 06h USB configuration 07h PCI configuration 08h Option ROM initialization 09h Video initialization 0Ah Cache initialization 0Ch Console input initialization 13h Starting Operating System

Table 4-29 BIOS Supported IPMI Events (continued)

Sensor	Event
Memory (0Ch)	Offset 00h Correctable ECC Offset 01h Uncorrectable ECC Offset 04h Memory Device Disabled Offset 05h Correctable ECC error logging limit reached Offset 06h Presence detected Offset 07h Configuration Error (Out of order) Event Data3: Bit — Description 0-3 — DIMM number 1..12 Fh DIMM number unknown 4 — DIMM number per Channel 0..1 5-6 — DIMM channel 0..2 7 — CPU Socket 0..1
Critical Interrupt (13h)	Offset 04h PCI PERR Offset 05h PCI SERR Event Data2: Bus number Event Data 3: Bit — Description 0-3 — PCI Function number 4-7 — PCI Device number
Boot Error (1Eh)	Offset 00h No bootable media (no boot device found)
Battery (29h)	Offset 01h Battery failed
System Firmware Progress (0Fh)	Offset 00h System Firmware Error 70h Front Panel Network not detected 78h Base Network not detected 79h Base Network reduced PCI performance 7Ah Base Network Device Error 80h Fabric Network not detected 81h Fabric Network reduced PCI performance 82h Fabric Network Device Error 88h Update Channel Network not detected 89h Update Channel Network reduced PCI performance 8Ah Update Channel Network Device Error 90h Reboot after a FRB2 Watchdog Timeout 91h Reboot after a BIOS/POST Watchdog Timeout 92h Reboot after a OS Load Watchdog Timeout 93h Reboot after a SMS/OS Watchdog Timeout 94h Reboot after a OEM Watchdog Timeout

4.12.4 SMBIOS Error Logging

The System Management BIOS (SMBIOS) Reference Specifications can be downloaded from http://www.dmtf.org/standards/smbios

The event log is a fixed length area in BIOS flash. Information about the SMBIOS event log area can be obtained from the DMI structure System Event Log Type 15. The DMI table can be read by the Linux tool dmidecode.

The "Log Change Token" in SMBIOS Type 15 structure is not supported.

The following SMBIOS Events are supported:

- Single-bit ECC memory error
- Multi-bit ECC memory error
- POST Error
- PCI Parity Error
- PCI System Error
- CPU Failure
- Correctable memory log disabled
- Log Area Reset/Cleared
- System boot
- OEM Event: "EFI Status code"

See *System Management BIOS (SMBIOS) Reference Specification Version: 2.7.0 Chapter 7.16.6.1 Event Log Types*.

4.12.4.1 Single-bit ECC Memory Error

This event is generated from the runtime error logging module. See *Runtime Error Logging* on page 121.

Table 4-30 Single-bit ECC Memory Error event format

Offset	Name	Format	Description
00h	Event Type	BYTE	Event Type = 01h
01h	Length	BYTE	always 0Ch
02h-07h	Date/Time Fields	BYTE	These fields contain the BCD representation of the date and time
08h-0Bh	Memory Information	UINT32	OEM extension

Table 4-31 Memory Information Definition

Bit	Description
0-7	reserved
8-15	DIMM number per Channel 0..1
16-23	DIMM channel 0..2
24-31	CPU Socket 0..1

4.12.4.2 Multi-bit ECC Memory Error

This event is generated from the runtime error logging module. See *Runtime Error Logging* on page 121.

Table 4-32 Multi-bit ECC Memory Error Event Format

Offset	Name	Format	Description
00h	Event Type	BYTE	Event Type = 02h
01h	Length	BYTE	always 0Ch

Table 4-32 Multi-bit ECC Memory Error Event Format (continued)

Offset	Name	Format	Description
02h-07h	Date/Time Fields	BYTE	These fields contain the BCD representation of the date and time
08h-0Bh	Memory Information	UINT32	OEM extension

Table 4-33 Memory Information Definition

Bit	Description
0-7	reserved
8-15	DIMM number per Channel 0..1
16-23	DIMM channel 0..2
24-31	CPU Socket 0..1

4.12.4.3 POST Error

If an error has occurred during the BIOS phase, a POST Error event is generated. There is only one POST Error event per boot generated.

A set bit at a Result DWORD bit position implies that the error associated with that position has occurred. If there was a error which has no corresponding bit in the Result DWORDs, the bit 0 form the Second DWORD is set (OEM: Unspecified Error).

Table 4-34 POST Error Event Format

Offset	Name	Format	Description
00h	Event Type	BYTE	Event Type = 02h
01h	Length	BYTE	Always 0Ch
02h-07h	Date/Time Fields	BYTE	These fields contain the BCD representation of the date and time
08h-0Bh	Result First DWORD	UINT32	See Table 4-35 on page 128
0Ch-0Fh	Result Second DWORD	UINT32	See Table 4-36 on page 128

Table 4-35 Result First DWORD supported POST Errors

Bit	Description
3	CMOS RAM Battery Failure. Battery is bad, removed or replaced
9	Keyboard Not Functional. No console input device found or device error
12	Memory Decreased in Size. DIMM errors during memory initialization found. Failed DIMM disabled
18	RTC Time Not Set. Found invalid Date/Time. Date/Time reset to a valid default value.
28	OEM: IPMI failure
29	OEM: IPMI Boot Parameter read/write error
30	OEM: IPMI Boot Parameter checksum error
31	OEM: IPMI Boot Parameter locked

Table 4-36 Result Second DWORD supported POST Errors

Bit	Description
0	OEM: unspecified error
1	OEM: North Bridge error
2	OEM: CPU error. This bit will be set additionally when a SMBIOS CPU Failure event is logged.
3	Front Panel Network Error
4	Base Network Error
5	Fabric Network Error
6	Update Channel Network Error
7	PCI Memory Conflict
17	Static Resource Conflict e.g. No Space for OPROM
19	System Board Device Resource Conflict
20	Primary Output Device Not Found
24	NVRAM Data Invalid. Flash write error

4.12.4.4 PCI Parity Error

This event is generated from the runtime error logging module. See *Runtime Error Logging* on page 121.

Table 4-37 PCI ParitY Error Event Format

Offset	Name	Format	Description
00h	Event Type	BYTE	Event Type = 09h
01h	Length	BYTE	Always 0Ch
02h-07h	Date/Time Fields	BYTE	These fields contain the BCD representation of the date and time
08h-0Bh	PCI Information	UINT32	OEM extension

PCI Information Definition:

Table 4-38 PCI Information Definition

Bit	Description
0-7	Reserved
8-15	PCI Function
16-23	PCI Device
24-31	PCI Bus number

4.12.4.5 PCI System Error

This event is generated from the runtime error logging module. See *Runtime Error Logging* on page 121.

Table 4-39 Multi-bit ECC Memory Error Event Format

Offset	Name	Format	Description
00h	Event Type	BYTE	Event Type = 0Ah
01h	Length	BYTE	Always 0Ch

Table 4-39 Multi-bit ECC Memory Error Event Format (continued)

Offset	Name	Format	Description
02h-07h	Date/Time Fields	BYTE	These fields contain the BCD representation of the date and time
08h-0Bh	PCI Information	UINT32	OEM extension

Table 4-40 Memory Information Definition

Bit	Description
0-7	Reserved
8-15	PCI Function
16-23	PCI Device
24-31	PCI Bus number

4.12.4.6 CPU Failure

This error is generated when a CPU Built In Self Test error has occurred.

Table 4-41 CPU Failure Event Format

Offset	Name	Format	Description
00h	Event Type	BYTE	Event Type = 0Bh
01h	Length	BYTE	Always 0Ch
02h-07h	Date/Time Fields	BYTE	These fields contain the BCD representation of the date and time

4.12.4.7 Correctable Memory Log Disabled

This event is generated from the runtime error logging module. It is logged when the Correctable Memory Error logging limit for the DIMM is reached. No further error events for this DIMM are logged.

See *Runtime Error Logging* on page 121.

Table 4-42 Correctable Memory Log Disabled Event Format

Offset	Name	Format	Description
00h	Event Type	BYTE	Event Type = 01h
01h	Length	BYTE	Always 0Ch
02h-07h	Date/Time Fields	BYTE	These fields contain the BCD representation of the date and time
08h-0Bh	Memory Information	UINT32	OEM extension

Table 4-43 Memory Information Definition

Bit	Description
0-7	Reserved
8-15	DIMM number per Channel 0..1
16-23	DIMM channel 0..2
24-31	CPU Socket 0..1

4.12.4.8 Log Area Reset/Cleared

This log entry is the first entry in the SMBIOS log.

Table 4-44 Log Area Reset/Cleared Event Format

Offset	Name	Format	Description
00h	Event Type	BYTE	Event Type = 16h
01h	Length	BYTE	Always 08h
02h-07h	Date/Time Fields	BYTE	These fields contain the BCD representation of the date and time

4.12.4.9 System Boot

This log entry is the first entry on a system boot.

Table 4-45 System Boot Event Format

Offset	Name	Format	Description
00h	Event Type	BYTE	Event Type = 17h
01h	Length	BYTE	Always 08h
02h-07h	Date/Time Fields	BYTE	These fields contain the BCD representation of the date and time

4.12.4.10 OEM Event EFI Status Code

EFI status codes are logged when "Convert OEM Codes" in "Smbios Event Log Settings" BIOS setup menu is set to disabled. In this case, no SMBIOS POST Error Event and no CPU Failure Events are generated.

Table 4-46 System Boot Event Format

Offset	Name	Format	Description
00h	Event Type	BYTE	Event Type = E0h
01h	Length	BYTE	Always 14h
02h-07h	Date/Time Fields	BYTE	These fields contain the BCD representation of the date and time
08h-0Bh	Status Code Type	UINT32	Error Code Severity
0Ch-0Fh	Status Code Value	UINT32	Error Code Value
10h-13h	Instance	UINT32	Additional Information e.g. DIMM Socket number

For a detailed description of the Status Code Type and the Status Code Value please refer to Intel Platform Innovation Framework for EFI Status Codes Specification Version 0.92. The specifications can be downloaded from http://www.intel.com/technology/framework/download.htm.

Table 4-47 Status Code Type Definition

Bit	Description
0-7	Type: 2 = Error Code
8-23	Reserved
24-31	Severity: 4 = Minor, 8 = Major

Table 4-48 Status Code Value Definition

Bit	Description
0-15	Operation code
16-23	SubClass code
24-31	Class code

Table 4-49 Class Code

Bit	Description
0h	Computing Unit
1h	Peripheral
2h	IO-Bus
3h	Software

4.12.4.10.1Artesyn OEM Extensions

Class Computing Unit:

Table 4-50 SubClass EFI_COMPUTING_UNIT_CHIPSET (06h)

Operation Code	Description
800Bh	Bad Battery

Table 4-50 SubClass EFI_COMPUTING_UNIT_CHIPSET (06h) (continued)

Operation Code	Description
800Dh	North Bridge Error

Table 4-51 SubClass EFI_COMPUTING_UNIT_FIRMWARE_PROCESSOR (02h) (IPMI)

Operation Code	Description
8100h	IPMI Boot Parameter USER area read error
8101h	IPMI Boot Parameter DEFAULT area read error
8102h	IPMI Boot Parameter USER area write error
8103h	IPMI Boot Parameter DEFAULT area write error
8104h	IPMI Boot Parameter USER area checksum error
8105h	IPMI Boot Parameter DEFAULT area checksum error
8106h	IPMI Boot Parameter USER area locked
8107h	IPMI Boot Parameter DEFAULT area locked

4.13 BIOS Status Codes

The following tables list the BIOS status codes applicable to the used AMI UEFI BIOS. The BIOS status codes are written to the blade's I/O Port 80 register and can be obtained by reading the "POST code" on-board IPMI sensor. The reading of the "POST code" sensor is only valid when the board is in the BIOS phase. The reading can be used to locate the cause of a board hang during BIOS phase. When the board has booted a OS, the reading of the '"POST code" sensor returns no valid status code.

4.13.1 Status Code Ranges

The following table contains details about Status Code Ranges.

Table 4-52 Status Code Ranges

Status Code Range	Description
0x01 – 0x0F	SEC Status Codes & Errors
0x10 – 0x2F	PEI execution up to and including memory detection
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0xCF	DXE execution up to BDS
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume errors (PEI)
0xE8 - 0xEF	Memory initialization errors
0xB0 - 0xBF	Additional Memory Initialization Status Codes
0xE8 - 0xEE	Additional Memory Error Status Codes

4.13.2 Standard Status Codes

The following tables contain details about the types of Status Codes.

Table 4-53 SEC Status Codes

Status Code	Description
0x0	Not used
Progress Codes	
0x1	Power on. Reset type detection (soft/hard).
0x2	AP initialization before microcode loading
0x3	North Bridge initialization before microcode loading
0x4	South Bridge initialization before microcode loading

Table 4-53 SEC Status Codes (continued)

Status Code	Description
0x5	OEM initialization before microcode loading
0x6	Microcode loading
0x7	AP initialization after microcode loading
0x8	North Bridge initialization after microcode loading
0x9	South Bridge initialization after microcode loading
0xA	OEM initialization after microcode loading
0xB	Cache initialization
SEC Error Codes	
0xC – 0xD	Reserved for future AMI SEC error codes
0xE	Microcode not found
0xF	Microcode not loaded

Table 4-54 PEI Status Codes

Status Code	Description
Progress Codes	
0x10	PEI Core is started
0x15	Pre-memory North Bridge initialization is started
0x19	Pre-memory South Bridge initialization is started
0x2F	Memory initialization (other)
0x31	Memory Installed
0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization)

Table 4-54 PEI Status Codes (continued)

Status Code	Description
0x37	Post-Memory North Bridge initialization is started
0x3B	Post-Memory South Bridge initialization is started
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started
Memory Initialization Codes	
0xB0	Chipset initialization
0xB1	Detect reset state
0xB2	DIMM detect
0xB3	Clock initialization
0xB4	Read SPD data
0xB5	early memory controller initialization
0xB6	Check DIMM population
0xB7	Channel initialization
0xB8	Channel training
0xB9	Run Build In Self Test
0xBA	Initialize memory map
0xBB	Setup RAS configuration
0xBF	Memory initialization complete
PEI Error Codes	
0x53	Memory initialization error. No usable memory detected
0x55	Memory not installed
0x56	Invalid CPU type or Speed
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error

Table 4-54 PEI Status Codes (continued)

Status Code	Description
0x5B	Reset PPI is not available
Memory Error Codes	
0xE8	No Memory
0xEA	DDR initialization error
0xEB	Memory test error
0xED	Mixed memory types
0xEE	Population error
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available
0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

Table 4-55 DXE Status Codes

Status Code	Description
0x60	DXE Core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started
0x68	PCI host bridge initialization

Table 4-55 DXE Status Codes (continued)

Status Code	Description
0x69	North Bridge DXE initialization is started
0x6A	North Bridge DXE SMM initialization is started
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization
0x78	ACPI module initialization
0x79	CSM initialization
0x80	IPMI Boot Parameter Initialization
0x81	Initialize Boot Variables
0x90	Boot Device Selection (BDS) phase is started
0x91	Driver connecting is started
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller Initialization
0x94	PCI Bus Enumeration
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console input devices connect
0x99	Super IO Initialization
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable

Table 4-55 DXE Status Codes (continued)

Status Code	Description
0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAB	Setup Input Wait
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)
DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources
0xD5	No Space for Legacy Option ROM
0xD6	No Console Output Devices are found
0xD7	No Console Input Devices are found

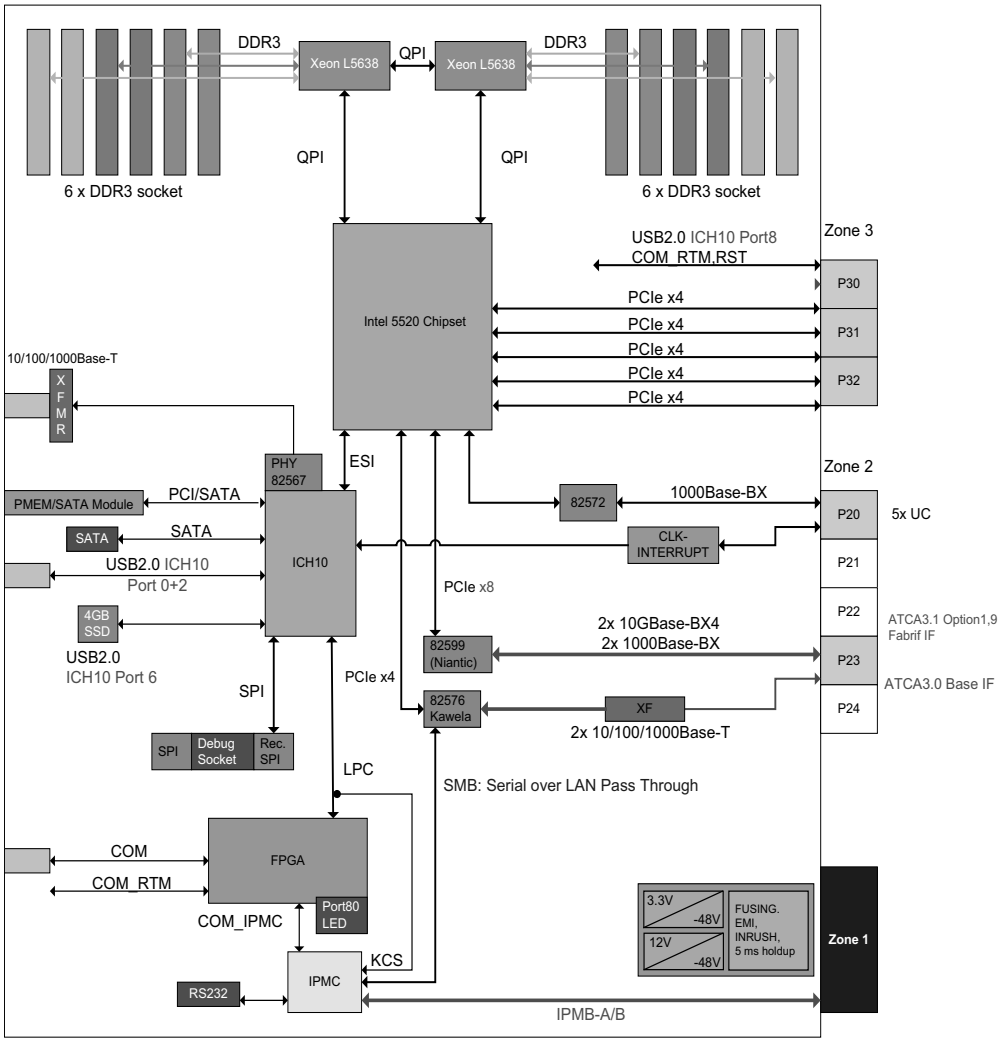
Table 4-55 DXE Status Codes (continued)

Status Code	Description
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available

5.1 Block Diagram

The following block diagram shows how the devices work together and how the data paths are used.

Figure 5-1 Block Diagram



5.2 Processor

ATCA-7365-CE provides either two Intel Xeon E5645 six-core processors or two Intel Xeon E5620 four-core processors as the central processing unit (CPU). Both CPUs are based on 32 nm process technology and provide the following main features:

- 2.4 GHz core frequency
- 32 KB instruction cache per core
- 32 KB L1 data cache per core
- 256 KB mid-level cache per core
- 12 MB L3 cache shared among the six cores

The processor features two Intel QuickPath Interconnect point-to-point links capable of up to 5.86 GT/s, 12 MB of shared Last Level cache (L3), and an Integrated Memory Controller (IMC). The processor supports all the existing Streaming SIMD Extensions 2 (SSE2), Streaming SIMD Extensions 3 (SSE3) and Streaming SIMD Extensions 4 (SSE4). The processor supports several Advanced Technologies: Execute Disable Bit, Intel 64 Technology, Enhanced Intel SpeedStep Technology, Intel Virtualization Technology (Intel VT), and Simultaneous Multi Threading (SMT).

5.3 Memory

The Xeon CPU features an integrated memory controller. The memory controller provides three memory channels that allow flexible memory configurations. DDR3 DIMM technology is exclusively supported. Different types of memory modules can be installed including registered DIMMs with ECC and un-buffered DIMMs with either ECC or non-ECC. The DIMM speeds can be either DDR3-800, DDR3-1066 or DDR3-1333 (not for E5620 processor). DIMMs of different speed selections can coexist, but the lowest speed selection will determine the used speed for all memory channels.

All processor variants support all the three memory clock speeds.

ATCA-7365-CE supports Low Voltage DDR3 (LVDDR3) Memory running at 1.35 V which reduces power consumption and improves thermal performance of the blade.

Either the normal DDR3 (1.5 V) or the LVDDR3 (1.35 V) can be used. Mixing is not possible.

5.3.1 Persistent memory (PMEM Module)

The blade supports a persistent memory. The persistent memory is an array of random access memory that preserves its contents during a payload reset. The memory is mapped into the memory address range of the CPU. Persistent memory is a necessary prerequisite for performing post mortem analysis of log data after reset and reboot of the payload CPU.

5.4 Chipset

The Intel 5520 chipset provides access between the two processors and the I/O subsystem. The chipset provides up to 36 PCI Express generation 2 lanes. The blade makes use of 5 times x4 PCIe lanes routed to the Zone 3 connector.

The chipset is connected to the ICH10R I/O Controller via the Enterprise Southbridge Interface (ESI).

5.5 I/O Controller

The ICH10R provides extensive I/O interface support and the BOOT path to SPI Boot Flash devices for the processor. ICH10R is connected to the system through the Enterprise Southbridge Interface (ESI) of the Xeon 5520 chipset.

The following is a list of the main internal features and the I/O interface functions provided by the ICH10R Southbridge.

- Six x4 PCI Express 1.1 Interface
- LPC interface
- SPI Interface (Boot Flash): up to two devices 20 + 33 MHz
- Six serial ATA (SATA) interfaces (2 used on ATCA-7365-CE)
- Twelve USB 2.0 interfaces (4 used on ATCA-7365-CE)
- Two 8259 Interrupt Controllers and I/O APIC controllers
- Integrated I/O APIC
- Power management support
- Two 8237 DMA controller

- 8254-based Counter Timer/timers
- High Precision Event Timers (HPET)
- RTC with 256-byte battery-backed SRAM
- System TCO (total cost of ownership) Reduction circuits
- SMBus interface
- Two stage Watchdog timer
- PCI 2.3 interface 32-bit/ 33 MHz (connects to PMEM module)
- General purpose I/O pins

ATCA-7365-CE does not provide a legacy Super-I/O device and no legacy Keyboard/Mouse interface. Keyboard and Mouse are supported through USB. Serial COM Interfaces are provided from FPGA.

5.6 Firmware Flashes

The blade has two physically separate 1 MB flash devices hosting the BIOS firmware:

- Primary (or Default BIOS) Flash (SPI0)
- Recovery BIOS Flash (SPI1)

The flash is allocated for storing the binary code of the BIOS. The ATCA-7365-CE boots from the primary flash SPI0 under normal circumstances. If booting BIOS from primary flash SPI0 fails, a hardware mechanism automatically changes the flash device select logic to boot from the recovery flash SPI1. The image that the processor will boot from after next reset is determined by the IPMC. It can be selected via dedicated IPMI OEM command.

5.7 Ethernet Ports

The blade utilizes various Ethernet controllers that serve the ATCA Base I/F, Fabric I/F, Update Channel and Ethernet console. All Ethernet interfaces have 1GbE capability except for the Fabric I/F controller which can operate at 10GbE or 1GbE (PICMG 3.1 Option 9 and 1). The fabric I/F is fully operable in both 10G and 1G mode without the presence of an RTM.

One Ethernet port is available on the front panel. Additional Ethernet ports for external access are provided via the RTM.

The Ethernet controllers support I/O virtualization.

Table 5-1 Ethernet Controller Types

Interface	Location	Controller	Count	Ethernet Type
Base Interface	P23	Intel 82576	2 x	10,100,1GB copper
Fabric Interface	P23	Intel 82599	2 x	10G/1G SerDes
Faceplate Interface	P27	Intel 82567	1 x	10,100,1 GB copper
Update Channel IF	P20	Intel 82572	1 x	1 GB SerDes

5.8 Storage Controller

Using an optional RTM, the blade provides a Serial Attached SCSI (SAS) controller. One on-board hard disk drive located on the RTM is connected to the controller. A minimum of two (2) ports are available on the RTM faceplate. They can be used to attach an external storage RAID (JBOD). Another SAS port of the controller is routed to ATCA Zone 3 for the purposes of synchronizing with a RTM based disk located in a logically paired ATCA slot.

5.9 Embedded Flash Disk

The ATCA-7365-CE blade, by default, provides an onboard USB Flash module (4GB) solid-state disk. The disk can keep data, application SW and OS boot images. Booting from the device is supported. The flash disk controller provides a wear leveling algorithm to improve the longevity of the flash device.

5.9.1 SATA Embedded Flash Solid State Disc (SSD)

As an option, a SATA embedded flash SSD solution can be provided through assembly of the ATCA-7365/SATA module which is available as an accessory kit.

5.10 BIOS

ATCA-7365-CE provides a BIOS firmware that is stored in flash memory. It can be updated remotely via Ethernet or locally via operating system. Along with the BIOS and BIOS Setup program, the flash memory contains POST and Plug and Play support.

The BIOS displays a message during POST identifying the type of BIOS and a revision code.

A BIOS extension is provided for the RTM based SAS controller to support RAID configuration.

5.11 IPMC

The Blade features an Intelligent Platform Management Controller (IPMC) compliant to PICMG 3.0 and IPMI 1.5 and 2.0 (SOL only). The IPMC is a management subsystem providing monitoring, event logging, and recovery control. The IPMC serves as the gateway for management applications to access the payload hardware.

The IPMC firmware (FW) is stored in two independent memory images. Crisis recovery control is provided to allow reboot of the IPMC from a 2nd image if the upgraded FW image is corrupted. FW images can be upgraded via HPM.1or IPMI using either IPMB or KCS interface.

The IPMC supports the initiation of a graceful shutdown of the host CPU. The IPMC can force the CPU to reset. It also controls the power and reset of the payload. As part of the power control logic circuitry is provided that controls the correct power-up and power-down sequencing of all payload specific power domains to prevent latch-up and damage of devices.

The IPMC provides a watchdog that supervises the payload. If enabled, the payload software needs to retrigger the Watchdog to prevent a time-out. A watchdog time-out can generate a NMI, a payload reset or disabling/cycling of the payload power. The watchdog settings, including enable/disable, can be changed by payload software (Setup menu). Time-out values can be selected from as short as seconds to as long as minutes.

The IPMC is supervised by a separate hardware Watchdog, which cannot be disabled. IPMC FW retriggers the Watchdog timer.

The IPMC monitors the Port 80 POST codes generated by the payload CPU. The IPMC is connected to various sensors on the Blade that provide temperature sensor readings at all major devices and voltage sensor readings of all major voltages. The IPMC monitors reset events caused by devices like Watchdog, IPMI command, and reset button.

The FRU information of the various modules including front board, RTM, and other modules can be read via the IPMC and if necessary upgraded through the IPMC.

The IPMC features Serial over LAN (SOL) for the payload CPU serial console. The SOL interface is available via the ATCA Base I/F. SOL is activated by specific IPMI commands.

5.12 Serial Redirection

The CPU serial redirection reroutes the console input and output; that is the text output to the text screen and input from the standard keyboard. The console typically is used by the BIOS setup menus, BIOS initialization and boot routines, OS boot loaders and loaded OSs.

The serial console of the payload CPU is available via SOL. In addition to the SOL capability the serial console is also available on the blade faceplate using a RJ45 connector with Cisco pin-out. If a SOL session is established, only the output is available on the faceplate. Input is not possible during this time via the faceplate. Alternatively to the CPU serial console, the IPMC serial console is also available on the faceplate serial connector. It can be selected via specific IPMI OEM command.

5.13 Serial over LAN

Serial Over LAN (SOL) enables suitably designed blades and servers to transparently redirect a serial character stream of a baseboard UART to/from a remote client via LAN over RMCP+ sessions. This enables users at remote consoles to access the serial port of a blade/server and interact with a text-based BIOS console, operating system, command line interfaces, and serial text-based applications.

The IPMC provides a dedicated sideband connection to the Base Interface Ethernet controller. This connectivity is not shared with IPMB-0 or any other I2C/SMBus/IPMB connections that the IPMC may use on the Blade for hardware management. Data from the payload serial redirection is routed through the sideband connection to the Base I/F. Vice versa the Ethernet controller filters packets based on either MAC address, RMCP port number, or IP address and forwards them to the serial redirection over the sideband interface. Alternatively, routing of SOL via PCIe may be considered if feasible by design.

Client software like openIPMI is required to enable SOL and to communicate with the SOL based serial console.

5.14 Control Logic

The Blade provides control logic for specific functions including:

- Payload power supervision and sequencing
- Payload resets
- Multiple HW interfaces between payload and IPMC
- Support for sensors as required

Any control circuitry based on programmable logic whether intended for payload supervision or as part of the payload is remotely upgradeable. Crisis recovery circuitry is provided to prevent board lock-ups as the result of a failed remote upgrade of the board control logic.

5.15 Front Board Faceplate

The blade's faceplate provides the following interfaces and control elements:

- Two USB 2.0 ports
- Serial console port to connect to either payload or IPMC serial I/F
- Out of Service, In Service, Attention, and Hot Swap LEDs
- One 1000Base-T Ethernet port
- Recessed reset button

The blade design provides the possibility to cover unused faceplate elements like LEDs or push button behind a custom overlay foil.

5.16 USB 2.0 Interface

The ICH10R provides internal USB1.1/ USB 2.0 host controllers with up to twelve USB 2.0 ports. Two ports are routed to the faceplate, one port is used on board to connect a USB 2.0 SSD User Flash Module and one port is routed to the RTM. The ports available at the faceplate are routed to a dual stacked connector. The ports are USB 2.0 compliant.

5.17 SMBus Interface

The SMBus interface of the ICH10R is connected to on-board devices like Clock PLLs, temperature sensors and the SPD PROMs of all twelve DDR3 DIMM memory modules. I^2C Bus Repeater of type PCA9515 is used to buffer the SMBus portion going to the SPD PROMs on the DIMM. The BIOS reads memory configuration parameters from SPD PROM. To address more than 8 memory I2C devices, the SMBus to the SPD PROMS is segmented.

Table 5-2 SMBus Devices

Device Name	Device Type	Address
SPD EEPROM	24C02	1010.000x b=A0
SPD EEPROM	24C02	1010.001x b=A2
SPD EEPROM	24C02	1010.010x b=A4
SPD EEPROM	24C02	1010.011x b=A6
SPD EEPROM	24C02	1010.100x b=A8
SPD EEPROM	24C02	1010.101x b=AA
SPD EEPROM	24C02	1010.000x b=A0
SPD EEPROM	24C02	1010.001x b=A2
SPD EEPROM	24C02	1010.010x b=A4
SPD EEPROM	24C02	1010.011x b=A6
SPD EEPROM	24C02	1010.100x b=A8
SPD EEPROM	24C02	1010.101x b=AA
Temp Sens#0	LM75	0x90
Temp Sens#1	LM75	0x92
DDR3 VREF_D margining	ISL90728	0x7C
DDR3 VREF_D margining	ISL90727	0x5C
Clock	ICS932S421	0xD2 + 0xD3
DB1200 clock	ICS9DB1200	0xDC + 0xDD
CK_MNG_133	ICS9FGP202	0xD0 + 0xD1
ICH10R Slave SMBus IF	ICH10R	0x88 + 0x89

Table 5-2 SMBus Devices (continued)

Device Name	Device Type	Address
Xeon 5520 (Tylersburg IOH36 D) Slave SMBus IF	Xeon 5520 (Tylersburg IOH36 D)	0xE0 (IOH Boostrap SMBUSID option is 0xC0)
MAX6618 PECI Hub	MAX6618	0x54

5.18 Real Time Clock

An external 32.768 kHz crystal sources the internal real time clock inside ICH10R with a frequency tolerance of 20 PPM. The RTC is fully DS1287, MC14618, PC87911, and Y2K compliant and provides 256 bytes of backed up CMOS RAM (of which 14 bytes containing the RTC time and date information and RTC configuration). During power-down, the RTC consumes 0.9uA/hr. The optional power-down backup method uses a Super CAP with a 1 Farad capacity. This provides 300 hours of RTC/SRAM backup. The default battery is an external +3V lithium battery with a capacity of 200mAh, which provides 3 years of backup.

5.19 VGA Module

The VGA-7360 module is based on XGI Volari Z11M graphics controller and delivers the following features on a standard DSUB 15 pin analog VGA graphics connector at the faceplate:

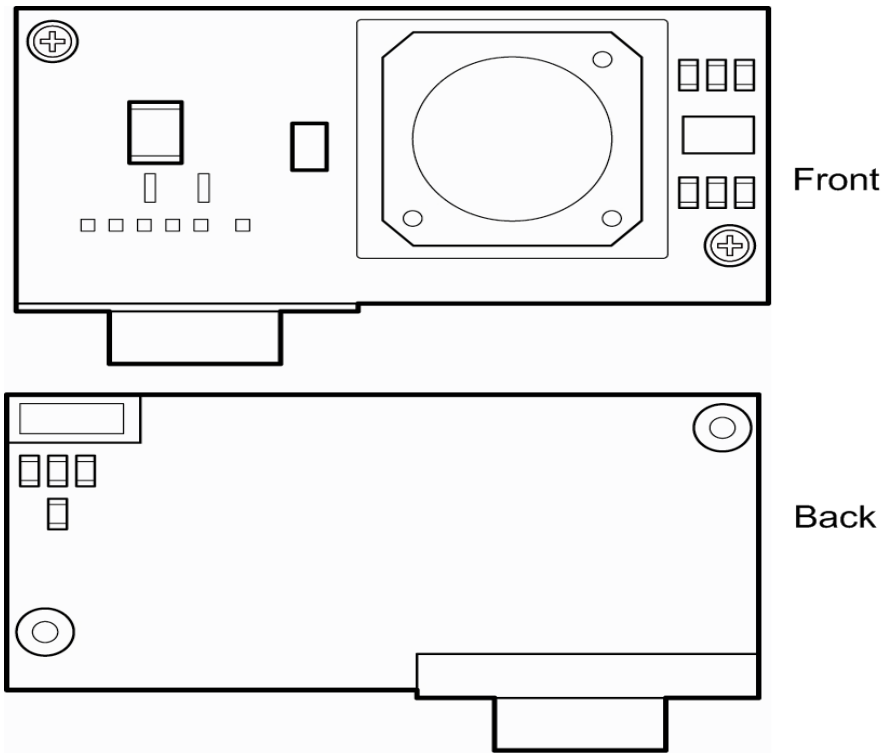
- High Performance 2D Accelerator
- 8 MB Integrated MCM Memory
- Analog CRT output with maximum 230 MHz pixel clock and graphics mode up to 1920x1200

One variant of ATCA-7365-CE supports the VGA-7360 module.

- ATCA-7365-24GB-V-CE

The faceplate for these variants are displayed in Figure 3-3 on page 67. The figure below shows the front and back views of the VGA-7360 module.

Figure 5-2 VGA-7360 Module (Front and Back View)



5.19.1 2D Graphics Engine

The Volari Z11M graphics controller incorporates a powerful 64-bit graphics engine to enhance the performance of 2D operations. The capabilities of the graphics engine include, but are not limited to BitBlt, Color Expansion, Enhanced Color Expansion, Line Drawing, Transparent BitBlt, and Rectangle Fill.

For all enhanced 256 color (8 bpp), 32k and 64k hi-color (16 bpp), and 16M true color (32 bpp) graphics modes, the 2D engine supports the following functions:

- 256 raster operations
- Rectangle fill
- Color expansion
- Enhanced Color expansion
- Line drawing with styled pattern
- Built-in bytes pattern registers
- Built-in 8x8 mask registers
- Rectangle Clipping
- Transparent BitBlt with source and destination keys
- Source data in command queue Bitblt

5.19.2 Supported VGA graphics modes

The Volari Z11M provides a 24-bit true color Digital-Analog-Converter (DAC). The maximum frequency of the RGB is 230 MHz. The maximum resolution the DAC supports is 1600x1200@60Hz video mode (16-bit high color) or 1280x1024@85Hz video mode (true color 32-bit). All Standard VGA modes are supported. The color palette, with 256 24-bit entries, converts a color code that specifies the color of a pixel into three 8-bit values, one each for red, green and blue. The 24-bit true color DAC is designed for direct color graphics mode. It converts each digital color value to three analog voltages for red, green, and blue.

6.1 Interrupt Structure

The ATCA-7365 supports NON-APIC (legacy PIC Mode) and APIC mode of Interrupt delivery to the CPUs. The 8259 PIC Mode Interrupt Concentrator inside the ICH10R supports 16 interrupts (eight external signal inputs). The IO-APIC device inside the ICH10R supports 24 interrupt sources. In APIC mode, the ICH10R supports only Front side bus interrupt delivery (not the serial APIC mode).

The following figure and tables summarize the interrupt sources and mappings for ATCA-7365. APIC mode is configured through BIOS after boot-up phase which is done in legacy PIC mode.

Figure 6-1 Interrupt Structure on ATCA-7365

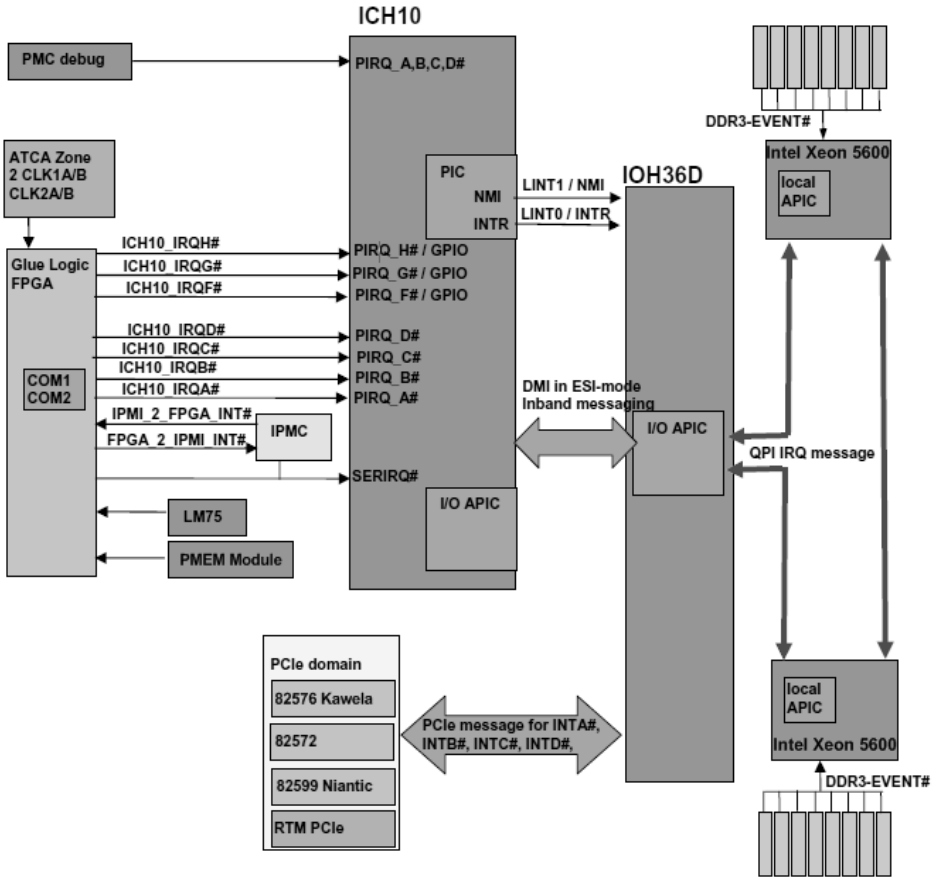


Table 6-1 APIC Mode Interrupt Mapping

IRQ	Interrupt Source
0	Cascade from 8259 1
1	
2	8254 Counter 0, Timer 0 (legacy mode)
3	
4	
5	
6	
7	
8	RTC, Timer 1 (legacy mode)
9	Option for TCI, TCO
10	Option for TCI, TCO
11	Timer 2, Option for TCI, TCO
12	Timer 3
13	FERR# logic
14	SATA Primary (legacy mode)
15	SATA Secondary (legacy mode)
16	PIRQ[A]#
17	PIRQ[B]#
18	PIRQ[C]#
19	PIRQ[D]#
20	PIRQ[E]# (GPIO)
21	PIRQ[F]# (GPIO)
22	PIRQ[G]# (GPIO)
23	PIRQ[H]# (GPIO)

In APIC Mode the PCI Interrupts A:H are mapped to IRQ[16:23]. If an Interrupt is used for PCI IRQ[A:H], SCI or TCO it must not be used for ISA (legacy)-style interrupts (via SERIRQ).

Table 6-2 Non-APIC (PIC mode/8259 Mode) Interrupt Mapping

	8259 IRQ	Typical Interrupt Source	Interrupt Source
Master	0	Internal	8254 Counter 0, Timer 0 (HPET)
	1	Keyboard	IRQ1 via SERIRQ
	2	Internal	Slave 8259 INTR output
	3	Serial Port A	IRQ3 via SERIRQ, PIRQ#
	4	Serial Port B	IRQ4 via SERIRQ, PIRQ#
	5	Parallel/Generic	IRQ5 via SERIRQ, PIRQ#
	6	Floppy	IRQ6 via SERIRQ, PIRQ#
	7	Parallel/Generic	IRQ7 via SERIRQ, PIRQ#
Slave	8	Internal RTC	Internal RTC, Timer 1 (HPET)
	9	Generic	IRQ9 via SERIRQ, SCI, TCO, or PIRQ#
	10	Generic	IRQ10 via SERIRQ, SCI, TCO, or PIRQ#
	11	Generic	IRQ11 via SERIRQ, SCI, TCO, or PIRQ# or Timer#2 (HPET)
	12	PS/2 Mouse	IRQ11 via SERIRQ, SCI, TCO, or PIRQ# or Timer#3 (HPET)
	13	Internal	State Machine output based on processor FERR# assertion. May optionally be used for SCI or TCO interrupt if FERR# not needed.
	14	SATA	SATA Primary (legacy mode), or via SERIRQ or PIRQ#
	15	SATA	SATA Secondary (legacy mode), or via SERIRQ or PIRQ#

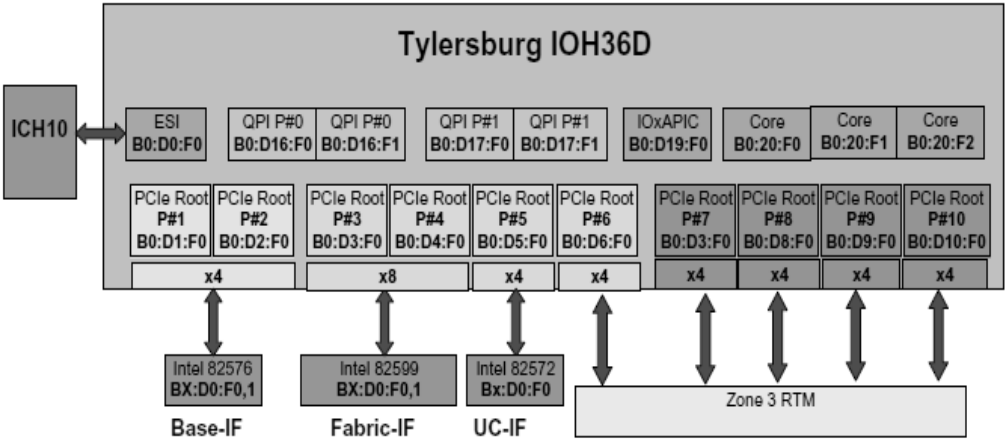
6.2 PCI Express Port Mapping

Xeon 5520 (Tylersburg IOH36 D) PCI Express ports have the naming convention as shown in Figure "IOH36D PCIe Port Mapping on ATCA-7365" on page 158.

Table 6-3 PCI Express Port Mapping

Port#	1	2	3	4	5	6	7	8	9	10
	x2	x2	x4	x4	x4	x4	x4	x4	x4	x4
	x4		x8		x8		x8		x8	
			x16				x16			

Figure 6-2 IOH36D PCIe Port Mapping on ATCA-7365



6.3 Registers

For register description, the convention is shown in Table "Register Default" on page 159 and Table "Register Access Type" on page 159.

Table 6-4 Register Default

Default	Description
-	Not applicable or undefined
0 or 1	Default value after PWR_GOOD is valid or after ICH_PLTRST deassertion.
Undef.	Undefined value
<reset>: 0 or 1	Default value after deassertion of the reset signal <reset>.
Ext.	External Reset Source. Default depends on external logic level.

Table 6-5 Register Access Type

Access	Description
r	Read only
w	Write only
r/w	Read and write
w1c	Write-1-to-clear, ignore bit while reading
r/w1c	Read and write-1-to-clear, write 0 has no effect
r/w1s	Read and write-1-to-set, write 0 has no effect
r/w1t	Read and write-1-to-toggle, write 0 has no effect
LPC:	The prefix “LPC:” signals that the access is restricted to the LPC interface. For example, LPC: r/w means that the register bit is read/writable from the LPC interface.
IPMC:	The prefix “IPMC:” signals that the access is restricted to the IPMC SPI interface. For example, IPMC: r/w means that the register bit is read/writable from IPMC SPI interface.

6.3.1 Register Decoding

The FPGA registers may be accessed from the host or the IPMC. The host uses the LPC bus interface and the IPMC uses an SPI interface.

6.3.1.1 LPC Decoding

The LPC bus supports different protocols.

6.3.1.1.1 LPC I/O Decoding

The LPC interface responds to LPC I/O accesses listed in Table "LPC I/O Register Map Overview" on page 160. All other LPC I/O accesses are ignored.

Table 6-6 LPC I/O Register Map Overview

Base Address	Address Size	Address Range Name	Description
0x4E	2	SIW	Super IO Configuration Registers for Index and Date
0x80	1	POSTCODE	POST Code Register
BASE1	8	COM1	UART1. Serial Port 1 (Logical Device 4). BASE1 address is set up during Super IO Configuration.
BASE2	8	COM2	UART2. Serial Port 2. (Logical Device 4). BASE2 address is set up during Super IO Configuration.
0x600	128	REGISTERS	FPGA Registers

All LPC I/O accesses to address POSTCODE, within the address range REGISTERS and within the address ranges of COM1 or COM2 (only when enabled during Super IO configuration) are decoded by the LPC core.

6.3.1.1.2 LPC Memory Decoding

The LPC interface never responds to LPC Memory accesses.

6.3.1.1.3 LPC Firmware Decoding

The LPC interface never responds to LPC Firmware accesses.

6.3.1.2 SPI Register Decoding

All SPI accesses from the IPMC towards the FPGA with the SPI select signal IPMC_SPI_SS_FPGA_ asserted are accepted.

Table 6-7 IPMC SPI Register

SPI Address Range	Address Range Name	Description
0x00 – 0x7F	REGISTERS	FPGA Registers

6.3.2 POST Code Register

The FPGA provides an 8-bit wide register to store POST codes to the LPC I/O address 0x80. The two nibbles of the register are converted to 7-segment codes and are displayed as two hex values by two 7-segment LED Displays.

The IPMC may read the POST code using the SPI interface (with the signal IPMC_SPI_SS_FPGA_ asserted) and the SPI address 0x7F.

Table 6-8 POST Code Register

LPC I/O Address: 0x80			
IPMC SPI Address: 0x7f			
Bit	Description	Default	Access
7:0	POST codes from host	0	LPC: r/w IPMC: r

6.3.3 Super IO Configuration Register

After a LPC Reset (ICH_PLTRST_ is asserted) or “Power On Reset” the Super IO is in the Run Mode with the UARTs disabled. They may be configured using the LPC IO Address Range SIW (INDEX and DATA) by placing the Super IO into Configuration Mode. The BIOS uses these configuration addresses to initialize the logical devices at POST. The INDEX and DATA addresses are only valid when the Super IO is in Configuration State. The INDEX and DATA addresses are effective only when the Super IO is in the Configuration State. When the Super IO is not in the Configuration State, reads return 0xFF and write data is ignored.

Table 6-9 Super IO Configuration Index Register

LPC I/O Address: 0x4E			
Bit	Description	Default	Access
7:0	INDEX. Configuration Index.	0xff	LPC: r/w

Table 6-10 Super IO Configuration Data Register

LPC I/O Address: 0x4F			
Bit	Description	Default	Access
7:0	DATA Configuration Data.	0xff	LPC: r/w

6.3.3.1 Entering the Configuration State

The device enters the Configuration State by the following contiguous sequence:

1. Write 68 to Configuration Index Port.
2. Write 08 to Configuration Index Port.

6.3.3.2 Configuration Mode

The system sets the logical device information and activates desired logical devices through the INDEX and DATA ports.

The desired configuration registers are accessed in two steps:

1. Write the index of the Logical Device Number Configuration Register (that is, 07) to the INDEX PORT and then write the number of the desired logical device to the DATA PORT.
2. Write the address of the desired configuration register within the logical device to the INDEX PORT and then write or read the configuration register through the DATA PORT.

If accessing the Global Configuration Registers, step (1) is not required. The Super IO returns to the RUN State.

Only two states are defined (Run and Configuration). In the Run State the Super IO is always ready to enter the Configuration State.

6.3.3.3 Super IO Configuration Registers

Address locations that are not listed are considered reserved register locations. Read operations to reserved registers may return non-zero values. Write operations to reserved locations may cause system failure.

6.3.3.3.1 Global Control Configuration Registers

The Super IO Global Registers lie in the address range 0x00-0x2F. All eight bits of the ADDRESS Port are used for register selection. All unimplemented registers and bits ignore writes and return zero when read. The INDEX PORT is used to select a configuration register in the chip. The DATA PORT is then used to access the selected register. These registers are accessible only in the Configuration Mode.

Table 6-11 Global Configuration Register Summary

Index Address	Description
0x07	Super IO Logical Device Number
0x20	Super IO Device ID
0x21	Super IO Device Revision
0x28	Super IO LPC
0x29	Super IO SERIRQ and Pre-divide Control

Table 6-12 Super IO Logical Device Number Register

Index Address: 0x07			
Bit	Description	Default	Access
7:0	Logical Device Number: 0x04: Logical Device 4 (UART 1Serial Port 1) 0x05: Logical Device 5 (UART2 Serial Port 2) A write to this register selects the current logical device. This allows access to the control and configuration registers for each logical device.	0	LPC: r/w

Table 6-13 Super IO Device Identification Register

Index Address: 0x20			
Bit	Description	Default	Access
7:0	Device ID	0	LPC: r

Table 6-14 Super IO Device Revision Register

Index Address: 0x21			
Bit	Description	Default	Access
7:0	Device Revision	0x01	LPC: r

Table 6-15 Super IO LPC Control Register

Index Address: 0x28			
Bit	Description	Default	Access
0	LPC Bus Wait States: 1: Long wait states (sync 6)	1	LPC: r
1	Reserved	0	LPC: r

Table 6-16 Global Super IO SERIRQ and Pre-divide Control Register

Index Address: 0x29			
Bit	Description	Default	Access
0	SERIRQ enable: 0: disabled. Serial interrupts disabled. 1: enabled. Logical devices participate in interrupt generations.	0	LPC: r/w
1	SERIRQ Mode: 1: Continuous Mode	1	LPC: r
3:2	UART Clock pre-divide 00: divide by 1 01: divide by 8 10: divide by 26 (CLK_UART is 48 MHz) 11: reserved	0	LPC: r/w
7:4	Reserved	0	LPC: r

6.3.3.3.2 Logical Device Configuration Registers

These are used to access the registers that are assigned to each logical unit. The Super IO supports two logical units and has two sets of logical device registers. The two logical devices are UART1 (Logical Number 4) and UART2 (Logical Number 5). A separate set (bank) of control and configuration registers exists for each logical device and is selected with the Logical Device Number Register. The INDEX PORT is used to select a specific logical device register. These registers are then accessed through the DATA PORT. The Logical Device registers are accessible only when the device is in the Configuration state.

Table 6-17 Logical Device Configuration Register Summary

Index Address	Description
0x30	Enable
0x60	Base IO Address MSB
0x61	Base IO Address LSB
0x70	Primary Interrupt Select
0x74	Reserved

Table 6-17 Logical Device Configuration Register Summary (continued)

Index Address	Description
0x75	Reserved
0xF0	Reserved

The logical register addresses are shown in the tables below.

Table 6-18 Logical Device Enable Register

Index Address: 0x30			
Bit	Description	Default	Access
0	Logical Device Enable: 0: disabled. Currently selected device is inactive. 1: enabled. The currently selected device is enabled.	1	LPC: r/w
7:1	Reserved	0	LPC: r

Table 6-19 Logical Device Base IO Address MSB Register

Index Address: 0x60			
Bit	Description	Default	Access
7:0	Logical Device Base IO Address MSB	0	LPC: r/w

Table 6-20 Logical Device Base IO Address LSB Register

Index Address: 0x61			
Bit	Description	Default	Access
2:0	Bits 0 to 2 are read only. Decode is on 8 Byte boundary.	0	LPC: r
7:3	Logical Device Base IO Address LSB. (Bits 3 to 7)		LPC: r/w

Registers 0x60 (MSB) and 0x61 (LSB) set the Logical Device Base IO for this logical device. For example for Base IO address 0x3F8 the content of Register 0x60 is 0x03 and the content of Register 0x61is 0xF8.

Refer the following table for Common Decode Ranges.

Table 6-21 Logical Device Common Decode Ranges

IO Address range	Description
0x3F8 – 0x3FF	COM1
0x2F8 – 0x2FF	COM2
0x2E8 – 0x2EF	COM3
0x3E8 – 0x3EF	COM4

Table 6-22 Logical Device Primary Interrupt Register

Index Address: 0x70			
Bit	Description	Default	Access
3:0	Interrupt level is used for Primary Interrupt. 0x0: No interrupt selected 0x1: IRQ1 0x2: IRQ2 0x3: IRQ3 0x4: IRQ4 0x5: IRQ5 0x6: IRQ6 0x7: IRQ7 0x8: IRQ8 0x9: IRQ9 0xA: IRQ10 0xB: IRQ11 0xC: IRQ12 0xD: IRQ13 0xE: IRQ14 0xF: IRQ15	1	LPC: r/w
7:4	Reserved	0	LPC: r

An Interrupt is activated by enabling this device (offset 0x30), setting this register to a non-zero value and setting any combination of bits 0-4 in the corresponding UART IER and the occurrence of the corresponding UART event (that is, Modem Status Change, Receiver Line Error Condition, Transmit Data Request, Receiver Data Available or Receiver Time Out) and setting the OUT2 bit in the MCR.

Table 6-23 Logical Device 0x74 Reserved Register

Index Address: 0x74			
Bit	Description	Default	Access
7:0	Reserved	0x04	LPC: r

Table 6-24 Logical Device 0x75 Reserved Register

Index Address: 0x75			
Bit	Description	Default	Access
7:0	Reserved	0x04	LPC: r

Table 6-25 Logical Device 0xF0 Reserved Register

Index Address: 0xF0			
Bit	Description	Default	Access
7:0	Reserved	0x04	LPC: r

6.3.4 UART1 and UART2 Register Map

The LPC IO Base addresses BASE1 for UART1 and BASE2 for UART2 are set up during Super IO configuration. Refer the section, *Super IO Configuration Registers* on page 163.

6.3.4.1 UART Register Overview

Table 6-26 on page 169 shows the registers and their addresses as offsets of a base address for one of the two UARTs.

The state of the Divisor Latch Bit (DLAB), which is the MOST significant bit of the Serial Line Control Register (SCR), affects the selection of certain of the UART registers. The DLAB bit must be set high by the system software to access the Baud Rate Generator Divisor Latches (DLL and DLM).

Table 6-26 UART Register Overview

LPC IO Address	DLAB Bit value	Description
Base	0	Receiver Buffer (RBR). Read Only
Base	0	Transmitter Holding (THR). Write Only.
Base + 1	0	Interrupt Enable Register (IER)
Base + 2	X	Interrupt Identification Register (IIR). Read Only
Base + 2	X	FIFO Control Register (FCR). Write Only.
Base + 3	X	Line Control Register (LCR)
Base + 4	X	Modem Control Register (MCR)
Base + 5	X	Line Status Register (LSR). Read Only
Base + 6	X	Modem Status Register (MSR). Read Only
Base + 7	X	Scratch Pad Register (SCR)
Base	1	Divisor Latch LSB (DLL)
Base + 1	1	Divisor Latch MSB (DLM)

6.3.4.2 UART Registers DLAB=0

6.3.4.2.1 Receiver Buffer Register (RBR)

In non-FIFO mode, this register holds the character received by the UART's Receive Shift Register. If less than eight bits are received, the bits are right-justified and the leading bits are zeroed. Reading the register empties the register and resets the Data Ready (DR) bit in the Line Status Register to zero. Other (error) bits in the Line Status Register are not cleared. In FIFO mode, this register latches the value of the data byte at the top of the FIFO.

Table 6-27 Receiver Buffer Register (RBR) if DLAB=0

LPC IO Address: Base			
Bit	Description	Default	Access
7:0	Receiver Buffer Register (RBR)	Undef.	LPC: r

6.3.4.2.2 Transmitter Holding Register (THR)

This register holds the next data byte to be transmitted. When the Transmit Shift Register becomes empty, the contents of the Transmit Holding Register are loaded into the shift register and the transmit data request (TDRQ) bit in the Line Status Register is set to one (1).

Table 6-28 Transmitter Holding Register (THR) if DLAB=0

LPC IO Address: Base			
Bit	Description	Default	Access
7:0	Transmitter Holding Register (THR)	Undef.	LPC: w

In FIFO mode, writing to THR puts data to the top of the FIFO. The data at the bottom of the FIFO is loaded to the shift register when it is empty.

6.3.4.2.3 Interrupt Enable Register (IER)

This register enables four types of interrupts which independently activate the int signal and set a value in the Interrupt Identification Register. Each of the four interrupt types can be disabled by resetting the appropriate bit of the IER register. Similarly, by setting the appropriate bits, selected interrupts can be enabled.

Table 6-29 Interrupt Enable Register (IER), if DLAB=0

LPC IO Address: Base + 1			
Bit	Description	Default	Access
0	Receive data interrupt enable/disable: 1: receive data interrupt enabled 0: receive data interrupt disabled	0	LPC: r/w
1	Transmitter holding register empty (THRE) interrupt enable/disable 1: THRE interrupt enabled 0: THRE interrupt disabled	0	LPC: r/w
2	Receiver line status interrupt enable/disable 1: receiver line status interrupt enabled 0: receiver line status interrupt disabled	0	LPC: r/w
3	Modem status interrupt enable/disable: 1: modem status interrupt enabled 0: modem status interrupt disabled	0	LPC: r/w
7:4	Reserved	0	LPC: r

6.3.4.2.4 Interrupt Identification Register (IIR)

In order to minimize software overhead during data character transfers, the UART prioritizes interrupts into four levels (listed in Table 6-30) and records these in the Interrupt Identification Register. The Interrupt Identification Register (IIR) stores information indicating that a prioritized interrupt is pending and the source of that interrupt.

Table 6-30 UART Interrupt Priorities

Priority Level	Interrupt Source
1 (highest)	Receiver Line Status. One or more error bits were set.
2	Received Data is available. In FIFO mode, trigger level was reached; in non-FIFO mode, RBR has data.
2	Receiver Time out occurred. It happens in FIFO mode only, when there is data in the receive FIFO but no activity for a time period.
3	Transmitter requests data. In FIFO mode, the transmit FIFO is half or more than half empty; in non-FIFO mode, THR is read already.
4	Modem Status. One or more of the modem input signals has changed state.

Table 6-31 Interrupt Identification Register (IIR)

LPC IO Address: Base + 1			
Bit	Description	Default	Access
0	Interrupt status bit: 1: no interrupt pending 0: interrupt pending	1	LPC: r
2:1	Interrupt priority level and source: 11: Receiver line status 10: Receiver data available 01: Transmitter holding register empty 00: Modem status	0	LPC: r
3	Time Out Detected: 0: No time out interrupt is pending 1: Character time-out indication (FIFO mode only)	0	LPC: r
5:4	Reserved	0	LPC: r

Table 6-31 Interrupt Identification Register (IIR) (continued)

LPC IO Address: Base + 1			
Bit	Description	Default	Access
7:6	FIFO Mode Enable bits: 00: Default mode 01: Reserved 10: Reserved 11: FIFO mode	0	LPC: r

6.3.4.2.5 FIFO Control Register (FCR)

FCR is a write-only register that is located at the same address as the IIR (IIR is a read-only register). FCR enables/disables the transmitter/receiver FIFOs, clears the transmitter/receiver FIFOs, and sets the receiver FIFO trigger level.

Table 6-32 FIFO Control Register (FCR)

LPC IO Address: Base + 2			
Bit	Description	Default	Access
0	FIFO enable/disable: 1: Transmitter and Receiver FIFO enabled 0: FIFO disabled	0	LPC: w
1	Receiver FIFO reset: 1: Bytes in receiver FIFO and counter are reset. Shift register is not reset (bit is self-clearing) 0: No effect	0	LPC: w
2	Transmit FIFO reset: 1: Bytes in receiver FIFO and counter are reset. Shift register is not reset (bit is self-clearing) 0: No effect	0	LPC: w
3	Receiver/Transmitter ready. Not supported.	0	LPC: w
5:4	Reserved	0	LPC: w

Table 6-32 FIFO Control Register (FCR) (continued)

LPC IO Address: Base + 2			
Bit	Description	Default	Access
7:6	Receiver FIFO interrupt trigger level: 00: 1 byte 01: 4 bytes 10: 8 bytes 11: 14 bytes	0	LPC: w

6.3.4.2.6 Line Control Register (LCR)

In the Line Control Register (LCR), the system programmer specifies the format of the asynchronous data communications exchange. The serial data format consists of a start bit (logic 0), five to eight data bits, an optional parity bit, and one or two stop bits (logic 1). The LCR has bits for accessing the Divisor Latch and causing a break condition. The programmer can also read the contents of the Line Control Register. The read capability simplifies system programming and eliminates the need for separate storage in system memory.

Table 6-33 Line Control Register (LCR)

LPC IO Address: Base + 3			
Bit	Description	Default	Access
1:0	Serial character WORD length: 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits	0	LPC: r/w
2	Stop bit length: 1: 1.5 stop bits for 5 bit WORD length 1: 2 stop bits for 6, 7, and 8 bit WORD length 0: 1 stop bit for any serial character WORD length	0	LPC: r/w

Table 6-33 Line Control Register (LCR) (continued)

LPC IO Address: Base + 3			
Bit	Description	Default	Access
3	Parity enable/disable When bit 3 is set, a parity bit is generated in transmitted data between the last data WORD bit and the first stop bit. In received data, if bit 3 is set, parity is checked. When bit 3 is cleared, no parity is generated or checked: 1: Parity enabled 0: Parity disabled	0	LPC: r/w
4	Parity even/odd When parity is enabled and bit 4 is set, even parity (an even number of logic ones in the data and parity bits) is selected. When parity is disabled and bit 4 is cleared, odd parity (an odd number of logic ones) is selected: 1: Even parity 0: Odd parity	0	LPC: r/w
5	Stick parity When bits 3, 4, and 5 are set, the parity bit is transmitted and checked as cleared. When bits 3 and 5 are set and bit 4 is cleared, the parity bit is transmitted and checked as set. If bit 5 is cleared, stick parity is disabled: 1: Stick parity enabled 0: Stick parity disabled	0	LPC: r/w
6	Break control bit Bit 6 is set to force a break condition, that is, a condition where TXD is forced to the spacing (cleared) state. When bit 6 is cleared, the break condition is disabled and has no affect on the transmitter logic. It only effects TXD: 1: Break condition enabled 0: Break condition disabled	0	LPC: r/w
7	Divisor latch access bit (DLAB) Bit 7 must be set to access the divisor latches of the baud generator during a read or write. Bit 7 must be cleared during a read or write to access the RBR, THR, or IER: 1: Access to DLL and DLM registers 0: Access to RBR, THR and IER registers	0	LPC: r/w

6.3.4.2.7 Modem Control Register (MCR)

This 8-bit register controls the interface with the modem or data set (or a peripheral device emulating a modem).

Table 6-34 Modem Control Register (MCR)

LPC IO Address: Base + 4			
Bit	Description	Default	Access
0	Data terminal ready (DTR#) output control: 1: DTR# output in low (active) state 0: DTR# output in high state	0	LPC: r/w
1	Request to send (RTS#) output control: 1: RTS# output in low (active) state 0: RTS# output in high state	0	LPC: r/w
2	User output control signal (OUT1#): 1: OUT1# output in high state 0: OUT1# output in low state Not supported	0	LPC: r/w
3	User output control signal (OUT2#): 1: OUT2# output in high state 0: OUT2# output in low state Not supported	0	LPC: r/w
4	Local loop back diagnostic control When loop back is activated: Transmitter TXD is set high. Receiver RXD is disconnected. Output of Transmitter Shift register is looped back into the receiver shift register input. Modem control inputs are disconnected Modem control outputs are internally connected to modem control inputs. Modem control outputs are forced to the inactive (high) levels: 1: Loop back mode activated 0: Normal operation	0	LPC: r/w

Table 6-34 Modem Control Register (MCR) (continued)

LPC IO Address: Base + 4			
Bit	Description	Default	Access
5	Autoflow control enable (AFE): 1: Autoflow control enabled (auto-RTS# and auto-CTS# or auto-CTS# only enabled) 0: Autoflow control disabled	0	LPC: r/w
7:6	Reserved	0	LPC: r

6.3.4.2.8 Line Status Register (LSR)

This register provides status information to the processor concerning the data transfers. Bits 5 and 6 show information about the transmitter section. The rest of the bits contain information about the receiver.

In non-FIFO mode, three of the LSR register bits, parity error, framing error, and break interrupt show the error status of the character that has just been received. In FIFO mode, these three bits of status are stored with each received character in the FIFO. LSR shows the status bits of the character at the top of the FIFO. When the character at the top of the FIFO has errors, the LSR error bits are set and are not cleared until software reads LSR, even if the character in the FIFO is read and a new character is now at the top of the FIFO.

Bits one through four are the error conditions that produce a receiver line status interrupt when any of the corresponding conditions are detected and the interrupt is enabled. These bits are not cleared by reading the erroneous byte from the FIFO or receive buffer. They are cleared only by reading LSR. In FIFO mode, the line status interrupt occurs only when the erroneous byte is at the top of the FIFO. If the erroneous byte being received is not at the top of the FIFO, an interrupt is generated only after the previous bytes are read and the erroneous byte is moved to the top of the FIFO.

Table 6-35 Line Control Register (LCR)

LPC IO Address: Base + 5			
Bit	Description	Default	Access
0	Receiver data ready (DR) indicator DR is set whenever a complete incoming character has been received and transferred into the RBR or the FIFO. DR is cleared by reading all of the data in the RBR or the FIFO: 1: New data received 0: No new data	0	LPC: r
1	Overrun error (OE) indicator When OE is set, it indicates that before the character in the RBR was read, it was overwritten by the next character transferred into the register. OE is cleared every time the CPU reads the contents of the LSR. If the FIFO mode data continues to fill the FIFO beyond the trigger level, an overrun error occurs only after the FIFO is full and the next character has been completely received in the shift register. An overrun error is indicated to the CPU as soon as it happens. The character in the shift register is overwritten but it is not transferred to the FIFO: 1: Overrun error occurred 0: No overrun error	0	LPC: r

Table 6-35 Line Control Register (LCR) (continued)

LPC IO Address: Base + 5			
Bit	Description	Default	Access
2	Parity Error (PE) indicator When PE is set, it indicates that the parity of the received data character does not match the parity selected in the LCR (bit 4). PE is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO: 1: Parity error occurred 0: No parity error	0	LPC: r
3	Framing Error (FE) indicator When FE is set, it indicates that the received character did not have a valid (set) stop bit. FE is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. The ACE tries to resynchronize after a framing error. To accomplish this, it is assumed that the framing error is due to the next start bit. The ACE samples this start bit twice and then accepts the input data: 1: Framing error occurred 0: No framing error	0	LPC: r
4	Break Interrupt (BI) indicator When BI is set, it indicates that the received data input was held low for longer than a full-word transmission time. A full-word transmission time is defined as the total time to transmit the start, data, parity, and stop bits. BI is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. When a break occurs, only one 0 character is loaded into the FIFO. The next character transfer is enabled after RXD goes to the marking state for at least two Receiver CLK samples and then receives the next valid start bit: 1: Full WORD transmission time exceeded 0: Normal operation	0	LPC: r

Table 6-35 Line Control Register (LCR) (continued)

LPC IO Address: Base + 5			
Bit	Description	Default	Access
5	Transmit Holding Register Empty (THRE) indicator THRE is set when the THR is empty, indicating that the ACE is ready to accept a new character. If the THRE interrupt is enabled when THRE is set, an interrupt is generated. THRE is set when the contents of the THR are transferred to the TSR. THRE is cleared concurrent with the loading of the THR by the CPU. In the FIFO mode, THRE is set when the transmit FIFO is empty; it is cleared when at least one byte is written to the transmit FIFO: 1: THR/Transmit FIFO empty 0: THR/Transmit FIFO contains data	0	LPC: r
6	Transmitter Empty (TEMT) indicator TEMT bit is set when the THR and the TSR are both empty. When either the THR or the TSR contains a data character, TEMT is cleared. In the FIFO mode, TEMT is set when the transmitter FIFO and shift register are both empty: 1: THR/Transmit FIFO/TSR empty 0: THR/Transmit FIFO/TSR contains data	0	LPC: r
7	FIFO data error In the FIFO mode, LSR7 is set when there is at least one parity, framing, or break error in the FIFO. It is cleared when the microprocessor reads the LSR and there are no subsequent errors in the FIFO. If FIFO is not used, bit always reads 0: 1: FIFO data error encountered 0: No FIFO error encountered	0	LPC: r

6.3.4.2.9 Modem Status Register (MSR)

This 8-bit register provides the current state of the control lines from the modem or data set (or a peripheral device emulating a modem) to the processor. In addition to this current state information, four bits of the Modem Status Register provide change information. Bits 03:00 are set to a logic 1 when a control input from the Modem changes state. They are reset to a logic 0 when the processor reads the Modem Status Register.

When bits 0, 1, 2, or 3 are set to logic 1, a Modem Status interrupt is generated if bit 3 of the Interrupt Enable Register is set.

Table 6-36 Modem Status Register (MSR)

LPC IO Address: Base + 6			
Bit	Description	Default	Access
0	Change in clear-to-send (DCTS) indicator DCTS indicates that the CTS# input has changed state since the last time it was read by the CPU. When DCTS is set (autoflow control is not enabled and the modem status interrupt is enabled), a modem status interrupt is generated. When autoflow control is enabled (DCTS is cleared), no interrupt is generated: 1: Change in state of CTS# input since last read 0: No change in state of CTS# input since last read	0	LPC: r/w
1	Change in data set ready (DDSR) indicator DDSR indicates that the DSR# input has changed state since the last time it was read by the CPU. When DDSR is set and the modem status interrupt is enabled, a modem status interrupt is generated: 1: Change in state of DSR# input since last read 0: No change in state of DSR# input since last read	0	LPC: r/w
2	Trailing edge of the ring indicator (TERI) detector TERI indicates that the RI# input to the chip has changed from a low to a high level. When TERI is set and the modem status interrupt is enabled, a modem status interrupt is generated. Not supported.	0	LPC: r/w
3	Change in data carrier detect (DDCD) indicator DDCD indicates that the DCD# input to the chip has changed state since the last time it was read by the CPU. When DDCD is set and the modem status interrupt is enabled, a modem status interrupt is generated. Not supported.	0	LPC: r/w
4	Complement of the clear-to-send (CTS#) input When the Asynchronous Communications Element (ACE) is in diagnostic test mode (LOOP [MCR4] = 1), this bit is equal to the MCR bit 1 (RTS#).	Ext.	LPC: r
5	Complement of the data set ready (DSR#) input When the ACE is in the diagnostic test mode (LOOP [MCR4] = 1), this bit is equal to the MCR bit 0 (DTR#).	Ext.	LPC: r

Table 6-36 Modem Status Register (MSR) (continued)

LPC IO Address: Base + 6			
Bit	Description	Default	Access
6	Complement of the ring indicator (RI#) input When the ACE is in the diagnostic test mode (LOOP [MCR4] = 1), this bit is equal to the MCR bit 2 (OUT1#). Not supported.	Ext.	LPC: r
7	Complement of the data carrier detect (DCD#) input When the ACE is in the diagnostic test mode (LOOP [MCR4] = 1), this bit is equal to the MCR bit 3 (OUT2#). Not supported.	Ext.	LPC: r

6.3.4.2.10 Scratch Register (SCR)

This 8-bit read/write register has no effect on the UART. It is intended as a scratch pad register for use by the programmer.

Table 6-37 Scratch Register (SCR))

LPC IO Address: Base + 7			
Bit	Description	Default	Access
7:0	Scratch Register (SCR) The scratch register is an 8 bit register that is intended for the programmer's use as a scratch pad in the sense that it temporarily holds the programmer's data without affecting any other ACE operation.	Undef.	LPC: r/w

6.3.4.3 Programmable Baud Rate Generator

The UART contains a programmable Baud Rate Generator that is capable of taking the UART_CLK input and dividing it by any divisor from 1 to (2 16 -1). The output frequency of the Baud Rate Generator is 16 times the baud rate. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization to ensure proper operation of the Baud Rate Generator. If both Divisor Latches are loaded with 0, the 16X output clock is stopped. Upon loading either of the Divisor latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load. Access to the Divisor latch can be done with a word write.

The UART_CLK is the CLK_UART (48MHz) input divided by the pre-divider set by the Super IO Configuration Register (Offset 0x29).

The baud rate of the data shifted in/out of the UART is given by:

Baud Rate = UART_CLK / (16X Divisor)

For example, if the pre-divider is 26 the UART_CLK is 1.8461538MHz. When the divisor is 12, the baud rate is 9600.

A Divisor value of 0 in the Divisor Latch Register is not allowed.

Table 6-38 Divisor Latch LSB Register (DLL), if DLAB=1

LPC IO Address: Base			
Bit	Description	Default	Access
7:0	Divisor Latch LSB (DLL)	Undef.	LPC: r/w

Table 6-39 Divisor Latch MSB Register (DLM), if DLAB=1

LPC IO Address: Base + 1			
Bit	Description	Default	Access
7:0	Divisor Latch MSB (DLM)	Undef.	LPC: r/w

6.4 FPGA Register Mapping

6.4.1 LPC I/O Register Map

The FPGA registers may be accessed via LPC I/O cycles in the I/O address range REGISTERS. See Table 6-40. For LPC register access, use the base address 0x600 and add the Address Offset. An LPC I/O write access to an address not listed in this table or not marked with an “X” in the LPC I/O column is ignored. A corresponding read access delivers always zero.

Note: LPC I/O Address = 0x600 + Address Offset

6.4.2 IPMC SPI Register Map

The FPGA registers may be accessed via IPMC SPI transactions (with the signal IPMC_SPI_SS_FPGA_ asserted). A SPI write access to an address not listed in this table or not marked with an “X” in the IPMC SPI column is ignored. A corresponding read access delivers always zero.

Table 6-40 FPGA Register Map Overview

Address Offset[1]	LPC I/O	IPMC SPI	Description
0x00	x	x	Module Identification Register
0x01	x	x	FPGA Version Register
0x03 - 0x05	x	x	Serial Line Routing Registers
0x06	x	x	IPMC Power Level Register
0x08	x	x	SPD PROM MUX Control Register
0x10	x	x	BIOS Reset Source Register
0x11	x	x	Reset Mask Register
0x12	x	x	BIOS IPMC Watch dog timeout Register
0x13	x	-	BIOS Push Button Enable Register
0x14	x	x	OS Reset Source Register
0x15	x	x	OS IPMC Watch dog timeout Register
0x16	-	x	IPMC Watch dog timeout Register
0x17	-	x	IPMC Reset Source Register
0x18 -0x19	x	-	RTM SPI Interface
0x20	x	-	External Interrupt Status Register
0x21	x	x	Processor Hot Status/Control Register
0x22	x	-	Telecom Status/Control Register
0x23 – 0x2D	x	-	Interrupt Mask and Map Registers
0x40	x	-	Flash Control and Status Register
0x41 – 0x42	x	-	Boot Flash Write Enable Registers
0x43	x	x	BIOS Boot Mode Register

Table 6-40 FPGA Register Map Overview (continued)

Address Offset[1]	LPC I/O	IPMC SPI	Description
0x45	x	x	SFMEM Module Configuration Register
0x48	x	x	Update Channel Equalization Control
0x49	x	-	IPMC E-Keying Status Register
0x4A	x	x	IPMC E-Keying Control Register
0x4B	x	-	IPMC GPIO Register
0x50	x	x	LED Status and Control Register
0x58	x	x	NMI Status and Control Register
0x60 -0x66	x	-	Telecom Clocking Registers
0x6F	x	x	Miscellaneous Status/Control Register
0x7D	x	x	LPC Scratch Register
0x7E	x	x	IPMC Scratch Register
0x7F	x	x	POST codes from host

1. For LPC I/O accesses add the LPC I/O Base Address 0x600

Note: For LPC I/O address, 0x80 is used.

6.4.3 Module Identification Register

The Module Identification Register identifies the ATCA-7365 Blade (Wellbeck).

Table 6-41 Module Identification Register

Address Offset: 0x00			
Bit	Description	Default	Access
7:0	ATCA-7365 Blade (Wellbeck) Module Identification	0x60	r

6.4.4 Version Register

The version register provides the version of the FPGA bit stream. The initial value starts at 0x01 and will be incremented with each new release.

Table 6-42 Version Register

Address Offset: 0x01			
Bit	Description	Default	Access
7:0	Specifies FPGA version	1 (Initial Value)	r

6.4.5 Serial Redirection Control Register

BIOS set the corresponding bit, which is used for serial redirection. The IPMC uses this information to route the corresponding port to serial IPMC interface in case of SOL.

BIOS should never set both status bits.

Table 6-43 Serial Redirection Control Register

Address Offset: 0x03			
Bit	Description	Default	Access
0	COM1 used for serial redirection: 0: COM1 not used for serial redirection 1: COM1 used for serial redirection	0	LPC: r/w IPMC: r
1	COM2 use for serial redirection 0: COM2 not used for serial redirection 1: COM2 used for serial redirection	0	LPC: r/w IPMC: r
7:2	Reserved	0	r

6.4.6 Serial over LAN (SOL) Control Register

The IPMC software can route serial data from serial port 1 (COM1) or serial port 2 (COM2) to the IPMC.

When both control bits are enabled, bit 1 is ignored.

Table 6-44 Serial over LAN Control Register

Address Offset: 0x04			
Bit	Description	Default	Access
0	SOL over COM1 enable: 0: disabled 1: enabled. COM1 is forwarded to IPMC	PWR_GOOD: 0	LPC: r/w IPMC: r
1	SOL over COM2 enable: 0: disabled 1: enabled. COM2 is forwarded to IPMC	PWR_GOOD: 0	LPC: r/w IPMC: r
7:2	Reserved	0	r

6.4.7 Serial Line Routing Register

The following table contains the Serial Line Routing Register details.

Table 6-45 Serial Line Routing Register

Address Offset: 0x05			
Bit	Description	Default	Access
1:0	Inverted level of signals SEL_SERIAL[1:0], which are controlled by switches SW2.2 and SW2.1. Switch setting may be overwritten by IPMC Software: 00: COM1 to Faceplate and COM2 to RTM 01: COM1 to RTM and COM2 to Faceplate 10: Reserved 11: Reserved	Ext. (SW2.2[1], SW2.1) 00: (OFF,OFF) 01: (OFF,ON) 10: (ON,OFF) 11: (ON,ON)	r
7:2	Reserved	0	r

1. The Signal SEL_SERIAL[1] is reserved. The switch SW2.2 should always be “OFF” and IPMC should not overwrite the default value.

6.4.8 IPMC Power Level Register

The following table contains the IPMC Power Level Register related information.

Table 6-46 IPMC Power Level Register

Address Offset: 0x06			
Bit	Description	Default	Access
7:0	IPMC Power Level. IPMC writes a value, which correspond to a defined power level.	PWR_GOOD:0	IPMC: r/w LPC: r

6.4.9 SPD PROM MUX Control Register

The following table contains the SPD PROM MUX Control Register information.

Table 6-47 SPD PROM MUX Control Register

Address Offset: 0x08			
Bit	Description	Default	Access
0	Signal Level of SMBUS_MUX0_IN	Ext.	r
1	Signal Level of SMBUS_MUX1_IN	Ext.	r
2	Signal Level of BIOS_POST_CMPLT_IN	Ext.	r
3	Reserved	0	r
4	SMBUS_MUX0_OUT.[1] 0: SMBUS_MUX0_OUT is driven low 1: SMBUS_MUX0_OUT is driven high	Ext.: SMBUS_MUX0_IN	LPC: r IPMC: r/w
5	SMBUS_MUX1_OUT. [2] 0: SMBUS_MUX1_OUT is driven low 1: SMBUS_MUX1_OUT is driven high	Ext.: SMBUS_MUX1_IN	LPC: r IPMC: r/w
6	BIOS_POST_CMPLT_OUT. [3] 0: BIOS_POST_CMPLT_IN is driven low 1: BIOS_POST_CMPLT_IN is driven high	Ext.: BIOS_POST_CMPLT_IN	LPC: r IPMC: r/w
7	SPD PROM MUX locked by BIOS 1: The output signals XXX_OUT are directly controlled by the corresponding input signals XXX_IN. 0: The output signals XXX_OUT are controlled by the corresponding bits 4 to 6.	0	LPC: r/w IPMC: r

1. When the SPD PROM MUX is locked by BIOS (Bit 7 is set) the signal level of SMBUS_MUX0_IN is read.Write transactions are ignored.

2. When the SPD PROM MUX is locked by BIOS (Bit 7 is set) the signal level of SMBUS_MUX1_IN is read. Write transactions are ignored.

3. When the SPD PROM MUX is locked by BIOS (Bit 7 is set) the signal level of BIOS_POST_CMPLT_IN is read. Write transactions are ignored.

6.4.10 Reset Registers

6.4.10.1 BIOS Reset Source Register

The BIOS Reset Source Register stores the source of the most recent reset. A one in the register bit indicates that the associated reset has occurred. If more than one reset occurs from different sources without clearing the corresponding register bits, one cannot determine the most recent reset source since more than one bit will be set. The same situation will happen, if two reset sources go active at the same time.

OS should never write to this register.

Table 6-48 BIOS Reset Source Register

Address Offset: 0x10			
Bit	Description	Default	Access
0	PWR_GOOD Payload Power-on reset 1: Reset occurred	PWR_GOOD:1	LPC: r/w1c IPMC: r
1	XDP0_BRD_PWROK CPU Debugger System reset request 1: Reset occurred	PWR_GOOD:0	LPC: r/w1c IPMC: r
2	PB_RST_ face plate push button reset 1: Reset occurred	PWR_GOOD:0	LPC: r/w1c IPMC: r
3	XDP1_DBRST_ CPU Debugger reset 1: Reset occurred	PWR_GOOD:0	LPC: r/w1c IPMC: r
4	RTM_PB_RST_ Reset key at RTM 1: Reset occurred	PWR_GOOD:0	LPC: r/w1c IPMC: r
5	CPU_RST_ CPU Reset signal from CPU 1: Reset occurred	PWR_GOOD:0	LPC: r/w1c IPMC: r
6	XDP0_DBRST_ CPU Debugger reset 1: Reset occurred	PWR_GOOD:0	LPC: r/w1c IPMC: r

Table 6-48 BIOS Reset Source Register (continued)

Address Offset: 0x10			
Bit	Description	Default	Access
7	IPMC_RST_ REQ_ Payload Reset from IPMC. 1: Reset occurred	PWR_GOOD:0	LPC: r/w1c IPMC: r

6.4.10.2 Reset Mask Register

The reset mask register enables or disables forwarding of a reset source to reset output signal. Only Push Button Resets requests are affected by the reset mask register. The register default values are latched when PWR_GOOD is asserted. This register can be read or written by the host CPU. A one in the register bit indicates that the associated reset is enabled. A zero indicates that the associated reset source is masked.

Table 6-49 Reset Mask Register

Address Offset: 0x11			
Bit	Description	Default	Access
0	Reserved	PWR_GOOD:1	r
1	Spare switch SW3.4	PWR_GOOD:0	r
2	PB_RST_ face plate push button reset 1: enabled 0: disabled	PWR_GOOD:0	r/w
3	Reserved	PWR_GOOD:0	r
4	RTM_PB_RST_ Reset key at RTM 1: enabled 0: disabled	PWR_GOOD:0	r/w
7:5	Reserved	PWR_GOOD:0	r

6.4.10.3 BIOS IPMC Watchdog Timeout Register

When one of the IPMC Watchdog Timeout: bit of IPMC Watchdog Timeout Register is set the corresponding BIOS IPMC Watchdog Timeout bit is set. The BIOS clears this status bit, writing one.

OS should never write to this register.

Table 6-50 BIOS IPMC Watchdog Timeout Register

Address Offset: 0x12			
Bit	Description	Default	Access
0	BIOS IPMC Watchdog Timeout: 1: IPMC Watchdog Timeout occurred	PWR_GOOD:0	LPC: r/w1c IPMC: r
1	BIOS IPMC Pre-Timeout 1: IPMC Pre-Timeout occurred	PWR_GOOD:0	LPC: r/w1c IPMC: r
7:2	Reserved	0	r

6.4.10.4 BIOS Push Button Enable Register

The BIOS needs to write to this register to enable the Front Panel push button reset, the RTM push button reset and the IPMC reset.

After a timeout of 8s the resets are armed again.

Table 6-51 BIOS Push Button Enable Register

Address Offset: 0x13			
Bit	Description	Default	Access
7:0	BIOS Push Button Enable Register	-	LPC: w

6.4.10.5 OS Reset Source Register

The OS Reset Source Register stores the source of the most recent reset as it is done in the BIOS Reset Source Register. A one in the register bit indicates that the associated reset has occurred. If more than one reset occurs from different sources without clearing the corresponding register bits, one cannot determine the most recent reset source since more than one bit will be set. The same situation will happen, if two reset sources go active at the same time.

BIOS should never write to this register.

Table 6-52 Reset Source Register

Address Offset: 0x14			
Bit	Description	Default	Access
0	PWR_GOOD Payload Power-on reset 1: Reset occurred	PWR_GOOD:1	LPC: r/w1c IPMC: r
1	XDP0_BRD_PWROK CPU Debugger System reset request 1: Reset occurred	PWR_GOOD:0	LPC: r/w1c IPMC: r
2	PB_RST_ face plate push button reset 1: Reset occurred	PWR_GOOD:0	LPC: r/w1c IPMC: r
3	XDP1_DBRST_ CPU Debugger reset 1: Reset occurred	PWR_GOOD:0	LPC: r/w1c IPMC: r
4	RTM_PB_RST_ Reset key at RTM 1: Reset occurred	PWR_GOOD:0	LPC: r/w1c IPMC: r

Table 6-52 Reset Source Register (continued)

Address Offset: 0x14			
Bit	Description	Default	Access
5	CPU_RST_ CPU Reset signal from CPU 1: Reset occurred	PWR_GOOD:0	LPC: r/w1c IPMC: r
6	XDP0_DBRST_ CPU Debugger reset 1: Reset occurred	PWR_GOOD:0	LPC: r/w1c IPMC: r
7	IPMC_RST_ REQ_ Payload Reset from IPMC. 1: Reset occurred	PWR_GOOD:0	LPC: r/w1c IPMC: r

6.4.10.6 OS IPMC Watchdog Timeout Register

When the IPMC Watchdog Timeout bit of IPMC Watchdog Timeout Register is set the OS IPMC Watchdog Timeout bit is set. The OS clears this status bit, writing one.

BIOS should never write to this register.

Table 6-53 OS IPMC Watchdog Timeout Register

Address Offset: 0x15			
Bit	Description	Default	Access
0	OS IPMC Watchdog Timeout: 1: IPMC Watchdog Timeout occurred	PWR_GOOD:0	LPC: r/w1c IPMC: r
1	OS IPMC Pre-Timeout 1: IPMC Pre-Timeout occurred	PWR_GOOD:0	LPC: r/w1c IPMC: r
7:2	Reserved	0	r

6.4.10.7 IPMC Watchdog Timeout Register

The IPMC SW set the corresponding bit to signal an IPMC watchdog timeout event. When the IPMC Watchdog Timeout bit is set from low to high, the corresponding bits in Table 6-50, BIOS IPMC Watchdog Timeout Register and Table 6-53, OS IPMC Watchdog Timeout Register are set.

IPMC needs to clear the IPMC watchdog timeout bit to arm IPMC watchdog timeout event recognition.

Table 6-54 IPMC Watchdog Timeout Register

Address Offset: 0x16			
Bit	Description	Default	Access
0	IPMC Watchdog Timeout: 0: No IPMC Watchdog Timeout 1: IPMC Watchdog Timeout occurred	PWR_GOOD:0	IPMC: r/w
1	IPMC Pre-Timeout 0: No IPMC Pre-Timeout 1: IPMC Pre-Timeout occurred	PWR_GOOD:0	IPMC: r/w
7:2	Reserved	0	r

6.4.10.8 IPMC Reset Source Register

The IPMC Reset Source Register stores the source of the most recent reset. A one in the register bit indicates that the associated reset has occurred. If more than one reset occurs from different sources without clearing the corresponding register bits, one cannot determine the most recent reset source since more than one bit will be set. The same situation will happen, if two reset sources go active at the same time.

Table 6-55 IPMC Reset Source Register

Address Offset: 0x17			
Bit	Description	Default	Access
0	PWR_GOOD Payload Power-on reset 1: Reset occurred	PWR_GOOD:1	IPMC: r/w1c
1	XDP0_BRD_PWROK CPU Debugger System reset request 1: Reset occurred	PWR_GOOD:0	IPMC: r/w1c
2	PB_RST_ face plate push button reset 1: Reset occurred	PWR_GOOD:0	IPMC: r/w1c
3	XDP1_DBRST_ CPU Debugger reset 1: Reset occurred	PWR_GOOD:0	IPMC: r/w1c
4	RTM_PB_RST_ Reset key at RTM 1: Reset occurred	PWR_GOOD:0	IPMC: r/w1c
5	CPU_RST_ CPU Reset signal from CPU 1: Reset occurred	PWR_GOOD:0	IPMC: r/w1c
6	XDP0_DBRST_ CPU Debugger reset 1: Reset occurred	PWR_GOOD:0	IPMC: r/w1c
7	IPMC_RST_ REQ_ Payload Reset from IPMC 1: Reset occurred	PWR_GOOD:0	IPMC: r/w1c

6.4.11 RTM SPI Interface Registers

The signals RTM_SPI_SCK, RTM_SPI_SS_, RTM_SPI_MISO and RTM_SPI_MOSI. are used to support a SPI master protocol. The signal RTM_SPI_MISO is used to signal the base board an ARTM interrupt. See *RTM Interrupt Status Register* on page 198.

At the moment there is no ARTM with an SPI interface defined.

A write access to the RTM SPI Address/Command Register starts the SPI transaction. The write access terminates, when SPI transaction has finished.

Table 6-56 RTM SPI Address/Command Register

Address Offset: 0x18			
Bit	Description	Default	Access
0	Command Bit 0: Write 1: Read	0	IPMC: r/w
7:1	RTM SPI Address bits [6:0]	PWR_GOOD:0	IPMC: r/w

A write access to the RTM SPI Address/Command Register with the Command Bit 0 (Write) starts a SPI write transaction. The value of the RTM SPI Write Register is written to the SPI device.

Table 6-57 RTM SPI Write Register

Address Offset: 0x19			
Bit	Description	Default	Access
7:0	RTM SPI write data	-	LPC: w

A write access to the RTM SPI Address/Command Register with the Command Bit 1 (Read) starts a SPI read transaction. The value of the RTM SPI Read Register contains the data read from the SPI device.

Table 6-58 RTM SPI Read Register

Address Offset: 0x19			
Bit	Description	Default	Access
7:0	RTM SPI read data	-	LPC: r

6.4.12 Interrupt Control and Status Registers

The interrupt status registers indicate the status of the interrupt input signals. They are read-only registers. When an interrupt is active the corresponding status bit is read 1. Write access to these register bits does not have any impact.

6.4.12.1 RTM Interrupt Status Register

The RTM Interrupt Status Register will be located in the RTM SPI address space. The host can access the RTM register using the RTM SPI Master Interface.

No RTM interrupt sources are defined yet.

6.4.12.2 External Interrupt Status Register

The following table shows the External Interrupt Status Register information.

Table 6-59 External Interrupt Status Register

Address Offset: 0x20				
Bit	Signal[1]	Description	Default	Access
0	IPMC2HOST_INT_	IPMC signals interrupt	Ext.	LPC: r
1	LM75_INT_	Interrupt input from payload Temp sensor	Ext.	LPC: r
2	SFMEM_IRQ_	Interrupt from SFMEM Module	Ext.	LPC: r
3	THERM_SEN0	IRQ request from 82599 Thermsen0	Ext.	LPC: r

Table 6-59 External Interrupt Status Register (continued)

Address Offset: 0x20				
Bit	Signal[1]	Description	Default	Access
4	THERM_SEN1	IRQ request from 82599 Thermsen1	Ext.	LPC: r
5	THERM_ALERT_	IRQ request from IOH Thermo-sensor	Ext.	LPC: r
6	APB_ALARM	An 48V input alarm (low voltage, etc)	Ext.	LPC: r
7	RTM_SPI_MISO	RTM interrupt sources 0: RTM_SPI_MISO is high. No RTM interrupt. 1: RTM_SPI_MISO is low. One or more RTM interrupt sources are active. When RTM SPI Master face is active the current level is latched.	Ext.	LPC: r

1. When an interrupt is active, the corresponding status bit is read 1.

6.4.12.3 Processor Hot Status/Control Register

The following table shows the Processor Hot Status/Control Register information.

Table 6-60 Processor Hot Status/Control Register

Address Offset: 0x21				
Bit	Signal	Description	Default	Access
0	CPU0_PRCHT_	IPMC signals interrupt	Ext.	LPC: r
1	CPU1_PRCHT_	Interrupt input from payload Temp sensor	Ext.	LPC: r
2	CPU0_PRCHT_	Interrupt from SFMEM Module	0	LPC: r/w
3	CPU1_PRCHT_	IRQ request from 82599 Thermsen0	0	LPC: r/w
7:4	-	Reserved	-	r

6.4.12.4 Telecom Status/Control Register

The following table shows the Telecom Status/Control Register details.

Table 6-61 Telecom Status/Control Register

Address Offset: 0x22				
Bit	Signal	Description	Default	Access
0	CH1_CLK1A_IN	Clock CLK1A of Chassis 1 has changed state from static to toggle or toggle to static.	0	LPC: r/w1c
1	CH1_CLK1B_IN	Clock CLK1A of Chassis 1 has changed state from static to toggle or toggle to static.	0	LPC: r/w1c
2	-	Telecom timeout occurred.	0	LPC: r/w1c
3	-	Reserved	-	r
7:4	-	Counter of Telecom timeout occurred. Clearing bit 2 of this register also clears this counter.	0	LPC: r

6.4.12.5 Interrupt Mask and Map Registers

Each interrupt signal of the External Interrupt Status Register, Processor Hot Status/Control Register or Telecom Status/Control Register can be mapped to one of the CPU_IRQ_X_ interrupt or any IRQ Frame number of the serialized IRQ protocol.

Multiple interrupt sources may share the same CPU_IRQ_X_ or the same IRQ Frame. In this case all interrupt sources need to be of type “level active low”.

Each Interrupt source has an Interrupt Mask and Map Register.

Table 6-62 Address Map of Interrupt Mask and Map Registers

Interrupt Source	Description	Address Offset of Interrupt Mask
IPMC2HOST_INT_	IPMC signals interrupt	0x23

Table 6-62 Address Map of Interrupt Mask and Map Registers (continued)

Interrupt Source	Description	Address Offset of Interrupt Mask
LM75_INT_	Interrupt input from payload Temp sensor	0x24
SFMEM_IRQ_	Interrupt from SFMEM Module	0x25
THERM_SEN0	IRQ request from 82599 Thermsen0	0x26
THERM_SEN1	IRQ request from 82599 Thermsen1	0x27
THERM_ALERT_	IRQ request from IOH Thermo-sensor	0x28
APB_ALARM	A 48V input alarm (low voltage, etc)	0x29
RTM_SPI_MISO	RTM interrupt sources	0x2A
CPU0_PRCHT_ CPU0	“Processor hot” interrupt	0x2B
CPU1_PRCHT_ CPU1	“Processor hot” interrupt	0x2C
Telecom Status/Control Register	Active when at least one Status bit (bit 0, 1 or 2) is set.	0x2D

Each Interrupt Mask and Map Register has the same layout. See the table below for more details.

The following table details the Interrupt Mask and Map Registers information.

Table 6-63 Interrupt Mask and Map Registers

Address Offset: 0x23 – 0x2D			
Bit	Description	Default	Access
4:0	IRQ Frame Number of Serialized IRQ protocol. Any valid Frame number enables interrupt. 0x00: Interrupt is mapped to CPU_IRQ_X_. See Bit 7:5 of this register. 0x01: Frame number 1. IRQ0 0x02: Frame number 2. IRQ1 0x03: Frame number 3. IRQ2 (SMI_) 0x04: Frame number 4. IRQ3 0x05: Frame number 5. IRQ4 0x06: Frame number 6. IRQ5 0x07: Frame number 7. IRQ6 0x08: Frame number 8. IRQ7 0x09: Frame number 9. IRQ8 0x0A: Frame number 10. IRQ9 0x0B: Frame number 11. IRQ1 0x0C: Frame number 12. IRQ11 0x0D: Frame number 13. IRQ12 0x0E: Frame number 14. IRQ13 0x0F: Frame number 15. IRQ14 0x10: Frame number 16. IRQ15 0x11: Frame number 17. IOCHK_ 0x12: Frame number 18. INTA_ 0x13: Frame number 19. INTB_ 0x14: Frame number 20. INTC_ 0x15: Frame number 21. INTD_ 0x16 – 0x1F: Frame number 22-31. IRQ Frame Number not valid. Value is ignored.	0	LPC: r/ w
7:5	An external Interrupt Signal CPU_IRQ_X_ is used. Only used when IRQ Frame Number is 0x00: 0x0: Interrupt is masked (disabled). 0x1: Map Interrupt to CPU_IRQ_A_ 0x2: Map Interrupt to CPU_IRQ_B_ 0x3: Map Interrupt to CPU_IRQ_C_ 0x4: Map Interrupt to CPU_IRQ_D_ 0x5: Map Interrupt to CPU_IRQ_F_ 0x6: Map Interrupt to CPU_IRQ_G_ 0x7: Map Interrupt to CPU_IRQ_H_	0	LPC: r/ w

6.4.13 Flash Status and Protection Registers

The flash status register indicates the actual status of the mechanical switches SW1.1 (Signal BOOT_DEF_WP_), SW1.2 (Signal BOOT_REC_WP_), SW1.3 (Signal BOOT_TSOP), SW3.1 (Signal BOOT_SEL_EN_) and SW3.2 (Signal BOOT_DEFAULT) and the status of IPMC signal BOOT_SELECT.

Table 6-64 Flash Status Register

Address Offset: 0x040			
Bit	Description	Default	Access
0	Default Boot SPI Flash Write protection Status. See Default Boot SPI Flash Write Enable register, how to disable write protection. 0: Default Boot SPI Flash is unprotected 1: Default Boot SPI Flash is protected	Ext. BOOT_DEF_WP_[1] 0: SW1.1 OFF 1: SW1.1 ON	LPC: r
1	Recovery Boot SPI Flash Write protection Status. See Recovery Boot SPI Flash Write Enable register, how to disable write protection 0: Recovery Boot SPI Flash is unprotected 1: Recovery Boot SPI Flash is protected	Ext. BOOT_REC_WP_[2] 0: SW1.2 OFF 1: SW1.2 ON	LPC: r
3:2	Reserved	0	LPC: r
4	TSOP or PLCC Boot select. Signal BOOT_TSOP. 0: TSOP selected 1: PLCC selected	Ext. 0: SW1.3 OFF 1: SW1.3 ON	LPC: r
5	Manual Boot Flash select enable. Signal BOOT_SEL_EN_. 0: Signal BOOT_SELECT selects active boot flash 1: Switch SW3.2 selects the active Boot Flash.	Ext. 0: SW3.1 OFF 1: SW3.1 ON	LPC: r
6	Manual Boot Flash select. Signal BOOT_DEFAULT. Used when SW3.1 is ON: 0: Selects Default Boot SPI Flash. 1: Selects Recover Boot SPI Flash.	Ext. 0: SW3.2 OFF 1: SW3.2 ON	LPC: r
7	IPMC signal BOOT_SELECT. Boot Flash Select. 0: Selects Default Boot SPI Flash 1: Selects Recovery Boot SPI Flash	Ext.	LPC: r

1. The default is latched from SW1.1 when ICH_PLTRST_ is deasserted.

2. The default is latched from SW1.2 when ICH_PLTRST_ is deasserted

Write protection status signals for the Boot SPI flashes are determined by external switch settings SW1.1and SW1.2. Software can overwrite the status of the write protection status by writing a magic word to the Boot SPI Flash Write Enable Registers.

Table 6-65 Default Boot SPI Flash Write Enable

Address Offset: 0x41			
Bit	Description	Default	Access
7:0	Default Boot SPI Flash Write enable/disable. A write value 0xC3 enables the Boot Block. All other values disable the Boot Block.	-	LPC: w

Table 6-66 Recovery Boot SPI Flash Write Enable

Address Offset: 0x42			
Bit	Description	Default	Access
7:0	Recovery Boot SPI Flash enable/disable. A write value 0xC3 enables the Flash. All other values disable the Flash.	-	LPC: w

6.4.14 BIOS Boot Mode Register

The following table provides details about BIOS Boot Mode Register.

Table 6-67 BIOS Boot Mode Register

Address Offset: 0x43			
Bit	Description	Default	Access
0	The switch signals SW_BIOS[1:0] controls the BIOS Boot Mode:	Ext. 1: SW4.3 ON 0: SW4.3 OFF	

Table 6-67 BIOS Boot Mode Register (continued)

Address Offset: 0x43					
Bit	Description			Default	Access
1	SW_BIOS[1:0]		BIOS BOOT MODE	Ext. 1: SW4.3 ON 0: SW4.3 OFF	r
	0 (OFF)	0 (OFF)	Normal BIOS execution (Default)		
	0 (OFF)	1 (ON)	BIOS Crisis recovery	Ext. 1: SW4.4 ON 0: SW4.4 OF	r
	1 (ON)	0 (OFF)	Load BIOS defaults		
	1 (ON)	1 (ON)	Port 80 codes to COM1		
7:2	Reserved			0	r

6.4.15 SFMEM Module Configuration Register

The following table provides details of SFMEM Module Configuration Register.

Table 6-68 SFMEM Module Configuration Register

Address Offset: 0x45			
Bit	Description	Default	Access
3:0	Control output signals SFMEM_CONF[3:0]	PWR_GOOD:0	LPC: r/w IPMC: r
7:4	Reserved	0	r

6.4.16 Update Channel Equalization Control Register

The following table provides information about Channel Equalization Control Register.

Table 6-69 Update Channel Equalization Control Register

Address Offset: 0x48			
Bit	Description	Default	Access
0	Control output Signal UC1_EQ_RX: 0: UC1_EQ_RX is driven low. 1: UC1_EQ_RX is tri-state.	0	LPC: r/w IPMC: r
1	Control output Signal UC1_EQ_TX: 0: UC1_EQ_TX is driven low. 1: UC1_EQ_TX is tri-state.	0	LPC: r/w IPMC: r
2	Control output Signal UC2_EQ_RX: 0: UC2_EQ_RX is driven low. 1: UC2_EQ_RX is tri-state.	0	LPC: r/w IPMC: r
3	Control output Signal UC2_EQ_TX: 0: UC2_EQ_TX is driven low. 1: UC2_EQ_TX is tri-state.	0	LPC: r/w IPMC: r
4	Control output Signal UC3_EQ_RX: 0: UC3_EQ_RX is driven low. 1: UC3_EQ_RX is tri-state.	0	LPC: r/w IPMC: r
5	Control output Signal UC3_EQ_TX: 0: UC3_EQ_TX is driven low. 1: UC3_EQ_TX is tri-state.	0	LPC: r/w IPMC: r
6	Control output Signal UC4_EQ_RX: 0: UC4_EQ_RX is driven low. 1: UC4_EQ_RX is tri-state.	0	LPC: r/w IPMC: r
7	Control output Signal UC4_EQ_TX: 0: UC4_EQ_TX is driven low. 1: UC4_EQ_TX is tri-state.	0	LPC: r/w IPMC: r

6.4.17 IPMC E-Keying Status Register

The following table provides information about IPMC E-Keying Status Register.

Table 6-70 IPMC E-Keying Status Register

Address Offset: 0x49			
Bit	Description	Default	Access
4:0	IPMC_UPDCH_[4:0]. IPMC electronic key signals	Ext.	LPC: r
5	IPMC_FAB1_10G_SEL_	Ext.	LPC: r
6	IPMC_FAB2_10G_SEL_	Ext.	LPC: r
7	Reserved	0	r

6.4.18 IPMC E-Keying Control Register

The following table provides information about IPMC E-Keying Control Register.

Table 6-71 IPMC E-Keying Control Register

Address Offset: 0x4A			
Bit	Description	Default	Access
0	Shut off the Intel82567 Faceplate GB Eth PHY. 0: FP_LAN_DISABLE_ driven low. Disabled 1: FP_LAN_DISABLE_ driven high. Enabled	1	LPC: r/w IPMC: r/w
1	Shut off the Intel8257x BASE-Eth Controller 0: BASEIF_DEV_OFF_ driven low. Device is OFF 1: BASEIF_DEV_OFF_ driven high. Device is ON	1	LPC: r/w IPMC: r/w
2	Enable/Disable Base-IF#1. 0: BASEIF_LAN0_DIS_ driven low. Disabled 1: BASEIF_LAN0_DIS_ driven high. Enabled	1	LPC: r/w IPMC: r/w
3	Enable/Disable Base-IF#2. 0: BASEIF_LAN1_DIS_ driven low. Disabled 1: BASEIF_LAN1_DIS_ driven high. Enabled	1	LPC: r/w IPMC: r/w

Table 6-71 IPMC E-Keying Control Register (continued)

Address Offset: 0x4A			
Bit	Description	Default	Access
4	Enable/Disable Fabric-IF#1. 0: FABIF_LAN0_DIS_ driven low. Disabled 1: FABIF_LAN0_DIS_ driven high. Enabled	1	LPC: r/w IPMC: r/w
5	Enable/Disable Fabric-IF#2. 0: FABIF_LAN1_DIS_ driven low. Disabled 1: FABIF_LAN1_DIS_ driven high. Enabled	1	LPC: r/w IPMC: r/w
6	Enable/Disable Update Channel ATCA Zone2 Port0. 0: UPDCIF_LAN_DIS_ driven low. Disabled 1: UPDCIF_LAN_DIS_ driven high. Enabled	1	LPC: r/w IPMC: r/w
7	Disable/Enable USB Port 8 to RTM. 0: RTMUSB_ENABLE_ driven low. Enabled 1: RTMUSB_ENABLE_ driven high. Disabled	PWR_GOOD: 1	LPC: r/w IPMC: r/w

6.4.19 IPMC GPIO Register

The following table provides information about IPMC GPIO Register.

Table 6-72 IPMC GPIO Register

Address Offset: 0x4B			
Bit	Description	Default	Access
0	IPMC_GPIO1	Ext.	LPC: r
1	IPMC_GPIO2	Ext.	LPC: r
2	IPMC_GPIO2	Ext.	LPC: r
7:3	Reserved		

6.4.20 LED Status and Control Register

The following table provides information about LED Status and Control Register.

Table 6-73 LED Status and Control Register

Address Offset: 0x50			
Bit	Description	Default	Access
0	Control green LED output Signal LED_GREEN_: 0: LED_GREEN_ is driven high. 1: LED_GREEN_ is driven low.	0	LPC: r/w IPMC: r
1	Control red LED output Signal LED_RED_: 0: LED_RED_ is driven high. 1: LED_RED_ is driven low.	0	LPC: r/w IPMC: r
2	Control user LED output Signal LED_USER1_: 0: LED_USER1_ is driven high. 1: LED_USER1 is driven low.	0	LPC: r/w IPMC: r
3	Control user LED output Signal LED_USER2_: 0: LED_USER2_ is driven high. 1: LED_USER2 is driven low.	0	LPC: r/w IPMC: r
5:4	Reserved	0	r
6	Signal level of ME_DISABLE_ (Connected to SW1.4 and ICH10 GP33)	Ext.	r
7	FPGA PROM select signal FPGA_PROM_SEL controlled by IPMC	Ext.	r

6.4.21 NMI Status and Control Register

The following table provides information about NMI Status and Control Register.

Table 6-74 NMI Status and Control Register

Address Offset: 0x58			
Bit	Description	Default	Access
0	Diagnostic NMI Status	0	LPC: r/w1c IPMC: r/w
1	Diagnostic NMI Status	0	LPC: r IPMC: r/w
2	Watchdog NMI Status	0	LPC: r/w1c IPMC: r/w
3	Watchdog NMI Status	0	LPC: r IPMC: r/w
7:4	Reserved	0	r

6.4.22 Telecom Clock Supervision Registers

6.4.22.1 Telecom Clocking Status Registers

The telecom backplane clocking status register indicates when the backplane input clock signals are toggling.

Table 6-75 Telecom Backplane Clocking Status Register

Address Offset: 0x66			
Bit	Description	Default	Access
0	0: CH1_CLK1A_IN is static or period is not in the correct range. 1: CH1_CLK1A_IN is toggling	PWR_GOOD:0	LPC: r
1	0: CH1_CLK1B_IN is static or period is not in the correct range. 1: CH1_CLK1B_IN is toggling	PWR_GOOD:0	LPC: r

Table 6-75 Telecom Backplane Clocking Status Register

Address Offset: 0x66			
Bit	Description	Default	Access
7:2	Reserved	0	r

Table 6-76 Telecom Backplane Clocking Latch Register

Address Offset: 0x67			
Bit	Description	Default	Access
7:0	Latch clock period measurements for CH1_CLK1A and CH1_CLK1B. Write data is discarded.	-	LPC: w

The Clock period of CH1_CLK1A is measured periodically. The result of the measurement (number of LPC clock cycles) is latched with a write access to the Telecom Backplane Clocking Latch Register. The 16 bit value is stored in the registers Telecom CH1_CLK1A clock period MSB Register and Telecom CH1_CLK1A clock period LSB Register. When the clock is static or the period is higher than a 16-bit value, the result is always 0xFFFF.

Table 6-77 Telecom CH1_CLK1A clock period MSB Register

Address Offset: 0x61			
Bit	Description	Default	Access
7:0	MSB of CH1_CLK1A clock period	PWR_GOOD: 0xFF	LPC: r

Table 6-78 Telecom CH1_CLK1A clock period LSB Register

Address Offset: 0x60			
Bit	Description	Default	Access
7:0	LSB of CH1_CLK1A clock period	PWR_GOOD: 0xFF	LPC: r

The Clock period of CH1_CLK1B is measured periodically. The result of the measurement (number of LPC clock cycles) is latched with a write access to the Telecom Backplane Clocking Latch Register. The 16-bit value is stored in the register Telecom CH1_CLK1B clock period MSB Register and Telecom CH1_CLK1B clock period LSB Register. When the clock is static or the period is higher than a 16-bit value, the result is always 0xFFFF.

Table 6-79 Telecom CH1_CLK1B clock period MSB Register

Address Offset: 0x63			
Bit	Description	Default	Access
7:0	MSB of CH1_CLK1B clock period	PWR_GOOD: 0xFF	LPC: r

Table 6-80 Telecom CH1_CLK1B clock period LSB Register

Address Offset: 0x62			
Bit	Description	Default	Access
7:0	LSB of CH1_CLK1B clock period	PWR_GOOD: 0xFF	LPC: r

6.4.22.2 Telecom Timer Registers

The Telecom Timer is decremented with each rising edge of the input clock.

The Telecom Timer is disabled when loaded with 0 (MSB and LSB Timer registers are 0). The Telecom Timer can be programmed from 1 to 65535, which allows timeout values from 125 micro seconds to 8.191875 sec (based on an 8kHz input clock).

When a timeout occurs (the timer is 0) the timeout bit is set. See Table 6-61 Telecom Status/Control Register. The Telecom Timer is reloaded with the timer start value stored in Telecom Timer LSB Register and Telecom Timer MSB Register and armed again, waiting for a rising edge of the input clock.

A write access to Telecom Timer MSB Register load the 16 bit Telecom timer with the write data of the current access and the content of the Telecom Timer LSB Register.

Table 6-81 Telecom Timer MSB Register

Address Offset: 0x65			
Bit	Description	Default	Access
7:0	MSB of Telecom Timer start value	PWR_GOOD: 0	LPC: r/w

Table 6-82 Telecom Timer LSB Register

Address Offset: 0x64			
Bit	Description	Default	Access
7:0	LSB of Telecom Timer start value	PWR_GOOD: 0	LPC: r/w

6.4.23 Miscellaneous Status/Control Registers

The following table provides information about Miscellaneous Status/Control Registers.

Table 6-83 CPLD Version and Spare Signal Status Register

Address Offset: 0x6F			
Bit	Description	Default	Access
2:0	CPLD Version. The CPLD uses the signals CPLD_SPARE[3:1]	Ext.	r
3	CPLD_SPARE[4]	Ext.	r
7:4	Reserved	0	r

6.4.24 Scratch Registers

The following table provides information about Scratch Registers.

Table 6-84 LPC Scratch Register

Address Offset: 0x45			
Bit	Description	Default	Access
7:0	LPC Scratch bits	PWR_GOOD:0	LPC: r/w IPMC: r

Table 6-85 IPMC Scratch Register

Address Offset: 0x45			
Bit	Description	Default	Access
7:0	IPMC Scratch bits	PWR_GOOD:0	LPC: r/w IPMC: r

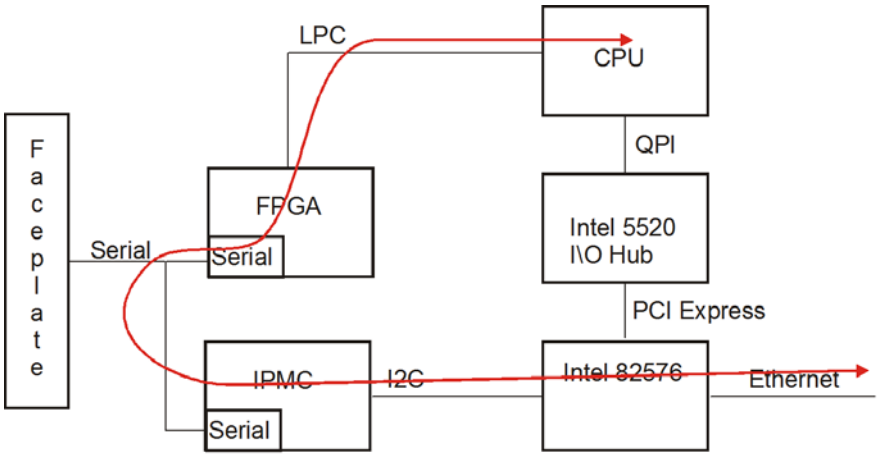
7.1 Overview

Serial Over LAN (SOL) is a mechanism that you can use to redirect the serial console from the blade via an IPMI session over the network. SOL uses the RMCP+ protocol.

The IPMC is used to establish and control the SOL session. SOL is only available on the base interface. The sideband interface of the Intel 82576 (in pass-through mode) is used to transmit/receive its terminal characters via the base interface.

Only a payload baud rate of 9600 baud is supported.

Figure 7-1 SOL Overview



You can configure the SOL parameters via standard IPMI commands or via an open source tool called "ipmitool".

7.2 Installing the ipmitool

You can download the open source ipmitool from http://ipmitool.sourceforge.net (at the time of publishing this manual the current version is 1.8.10). Documentation for this tool is also freely available on this site.

Procedure

To install the ipmitool, proceed as follows.

1. Download the ipmitool tar file from http://ipmitool.sourceforge.net to your blade.
2. Extract the source code.
   ```
   prompt>tar -xjvf ipmitool-<version>.tar.bz2
   ```
3. Go to the directory to which you have extracted the ipmitool.
   ```
   prompt>cd <path>/ipmitool-<version>
   ```
4. Build the ipmitool.
   ```
   prompt>./configure && make && make install
   ```

7.3 Configuring SOL Parameters

You can configure the following SOL parameters.

Table 7-1 SOL Parameters

Parameter	Description
Set LAN Configuration Parameter (IP address/MAC address)	Use this command to set the IP and MAC address.
Set Channel Access (Privilege level)	Use this command to set the privilege level.
Set User Name	Default value is *soluser*
Set User Password	Default value is *solpasswd*

You can use standard IPMI commands or the ipmitool to modify the parameters.

7.3.1 Using Standard IPMI Commands

This example shows how to setup the SOL configuration parameter with standard IPMI commands. Ipmicmd is used on the local IPMC and the IP is configured.

Sample Procedure

To set the IP address, proceed as follows:

1. Establish an IPMI connection to the blade.
2. Set LAN Configuration Parameter Set In Progress Lock.
   ipmicmd -k "f 0 c 1 5 0 1" smi 0
3. Set LAN Configuration Parameter Set IP (172.16.10.11 on channel 5).
   ipmicmd -k "f 0 c 1 5 3 ac 10 0a dd" smi 0
4. Set LAN Configuration Parameter Set In Progress Commit.
   ipmicmd -k "f 0 c 1 5 0 2" smi 0

7.3.2 Using ipmitool

The example below shows how to setup a LAN configuration parameter for a potential SOL session with ipmitool for Base Ethernet Channel 1 (channel 5).

```
n0s70:~ #ipmitool lan set 5 ipaddr 172.16.0.221

Setting LAN IP Address to 172.16.0.221

n0s70:~ #
```

The following example shows how to query the LAN parameters that are currently in use for a potential SOL session for Base Ethernet Channel 1 (channel 5) and Base Ethernet Channel 2 (channel 6):

```
root@localhost:~# ipmitool lan print 5

Set in Progress         : Set Complete

Auth Type Support       :

Auth Type Enable        : Callback :

                        : User     :

                        : Operator :
```

```
                          : Admin    :
                          : OEM      :
IP Address Source         : Unspecified
IP Address                : 172.16.0.221
Subnet Mask               : 255.255.0.0
MAC Address               : 00:00:00:00:00:00
Default Gateway IP        : 172.16.0.1
Default Gateway MAC       : 00:00:00:00:00:00
RMCP+ Cipher Suites       : 1,2,3,3
Cipher Suite Priv Max     : Not Available
root@localhost:~# ipmitool lan print 6
Set in Progress           : Set Complete
Auth Type Support         :
Auth Type Enable          : Callback :
                          : User     :
                          : Operator :
                          : Admin    :
                          : OEM      :
IP Address Source         : Unspecified
IP Address                : 172.17.1.220
Subnet Mask               : 255.255.0.0
MAC Address               : 00:00:00:00:00:00
Default Gateway IP        : 172.17.0.1
```

```
Default Gateway MAC      : 00:00:00:00:00:00
RMCP+ Cipher Suites      : 1,2,3,3
Cipher Suite Priv Max    : Not Available
root@localhost:~#
```

MAC Address 00:00:00:00:00:00 means the address is shared between base and SOL interface. The address can be found out in the MAC address record of the FRU.

7.4 Establishing a SOL Session

To start an SOL session, the following requirements must be fulfilled:

- An Ethernet LAN connection to the 82576 controller of the ATCA-7365-CE must exist.
- ATCA-7365-CE IPMC FW must correspond to version 2.00.7 and above.

Procedure

To establish a SOL session, proceed as follows:

1. Make sure that the requirements detailed above are fulfilled.
2. Compile and install the ipmitool on your target which is destined for opening the SOL session on the ATCA-7365-CE. For details refer to *Installing the ipmitool* on page 215.
3. Apply an IP address to the ATCA-7365-CE SOL interface - for details refer to *Configuring SOL Parameters* on page 216.
4. If necessary change user and password.
   Default user is "soluser" and password is "solpasswd".
5. Configure the network between the ATCA-7365-CE and your target, which is destined for opening the SOL session, so that the SOL IP address is accessible.

6. Start ATCA-7365-CE SOL session on your target with the ipmitool and the configured IP address for the ATCA-7365 SOL interface.
   `ipmitool -C 1 -I lanplus -H 172.16.0.221 -U soluser -P solpasswd -k gkey sol activate`
   For details on the command parameters, refer to the ipmitool documentation available on http://ipmitool.sourceforge.net.

To access BIOS setup screen, it is necessary to reset the payload. SOL session is only available if the payload is powered on and initialized by the BIOS.

Supported IPMI Commands

8.1 Standard IPMI Commands

The IPMC is fully compliant to the Intelligent Platform Management Interface v1.5. This section provides information about the supported IPMI commands.

8.1.1 Global IPMI Commands

The IPMC supports the following global IPMI commands.

Table 8-1 Supported Global IPMI Commands

Command	NetFn (Request/Response)	CMD	Comments
Get Device ID	0x06/0x07	0x01	-
Cold Reset	0x06/0x07	0x02	-
Warm Reset	0x06/0x07	0x03	-
Get Self Test Results	0x06/0x07	0x04	-
Get Device GUID	0x06/0x07	0x08	-
Master Write-Read	0x06/0x07	0x52	Only for accessing private I2C buses.

8.1.2 System Interface Commands

The system interface commands are supported by blades providing a system interface.

Table 8-2 Supported System Interface Commands

Command	NetFn (Request/Response)	CMD
Set BMC Global Enables	0x06/0x07	0x2E
Get BMC Global Enables	0x06/0x07	0x2F
Clear Message Flags	0x06/0x07	0x30
Get Message Flags	0x06/0x07	0x31
Get Message	0x06/0x07	0x33
Send Message	0x06/0x07	0x34

Table 8-2 Supported System Interface Commands (continued)

Command	NetFn (Request/Response)	CMD
Set Channel Access	0x06/0x07	0x40
Get Channel Access	0x06/0x07	0x41
Get Channel Info	0x06/0x07	0x42
Set User Access	0x06/0x07	0x43
Get User Access	0x06/0x07	0x44
Set User Name	0x06/0x07	0x45
Get User Name	0x06/0x07	0x46
Set User Password	0x06/0x07	0x47
Set User Payload Access	0x06/0x07	0x4C
Get User Payload Access	0x06/0x07	0x4D
Set Channel Security Keys	0x06/0x07	0x5C

8.1.3 Watchdog Commands

The watchdog commands are supported by blades providing a system interface and a watchdog type 2 sensor.

The options pre-timeout and power-cycle are not supported.

Table 8-3 Supported Watchdog Commands

Command	NetFn (Request/Response)	CMD
Reset Watchdog Timer	0x06/0x07	0x22
Set Watchdog Timer	0x06/0x07	0x24
Get Watchdog Timer	0x06/0x07	0x25

8.1.4 SEL Device Commands

The following table describes the SEL Device Commands information.

Table 8-4 Supported SEL Device Commands

Command	NetFn (Request/Response)	CMD
Get SEL Info	0x0A/0x0B	0x40
Reserve SEL	0x0A/0x0B	0x42
Get SEL Entry	0x0A/0x0B	0x43
Add SEL Entry	0x0A/0x0B	0x44
Clear SEL	0x0A/0x0B	0x47
Get SEL Time	0x0A/0x0B	0x48
Set SEL Time	0x0A/0x0B	0x49

8.1.5 FRU Inventory Commands

The following table describes the FRU Inventory Commands information.

Table 8-5 Supported FRU Inventory Commands

Command	NetFn (Request/Response)	CMD
Get FRU Inventory Area Info	0x0A/0x0B	0x10
Read FRU Data	0x0A/0x0B	0x11
Write FRU Data	0x0A/0x0B	0x12

8.1.6 Sensor Device Commands

The following table describes the Sensor Device Commands information.

Table 8-6 Supported Sensor Device Commands

Command	NetFn (Request/Response)	CMD	Comments
Get Device SDR Info	0x04/0x05	0x20	-
Get Device SDR	0x04/0x05	0x21	-
Reserve Device SDR Repository	0x04/0x05	0x22	-
Get Sensor Reading Factors	0x04/0x05	0x23	-
Set Sensor Hysteresis	0x04/0x05	0x24	-
Get Sensor Hysteresis	0x04/0x05	0x25	-
Set Sensor Threshold	0x04/0x05	0x26	Most of the threshold-based sensors have fixed thresholds. Before using this command, check whether threshold setting is supported by using the Get Device SDR command.
Get Sensor Threshold	0x04/0x05	0x27	-
Set Sensor Event Enable	0x04/0x05	0x28	-
Get Sensor Event Enable	0x04/0x05	0x29	-
Get Sensor Event Status	0x04/0x05	0x2B	-
Get Sensor Reading	0x04/0x05	0x2D	-
Get Sensor Type	0x04/0x05	0x2F	-
Set Event Receiver	0x04/0x05	0x00	-
Get Event Receiver	0x04/0x05	0x01	-
Platform Event	0x04/0x05	0x02	-

8.1.7 Chassis Device Commands

The following table details Chassis Device Commands information.

Table 8-7 Supported Chassis Device Commands

Command	NetFn (Request/Response)	CMD
Set System Boot Options	0x00/0x01	0x08
Get System Boot Options	0x00/0x01	0x09

8.1.7.1 System Boot Options Commands

The IPMI system boot options commands allow you to control the boot process of a blade by sending boot parameters to the blade's boot firmware (for example BIOS, U-Boot or VxWorks). The boot firmware interprets the sent boot parameters and executes the boot process accordingly. Each boot parameter addresses a particular functionality and consists of a sequence of one or more bytes. The IPMI specification assigns numbers to boot parameters. Boot parameters 0 to 7 are standard parameters whose structure and functionality is defined by the IPMI specification. The boot parameters 96 to 127 are OEM-specific which can be used for different purposes.

When using the Get/Set System Boot Options commands, except for parameter 100, use the response/request data fields with the Set Selector and the Block Selector set to 0x00. When using the Get/Set System Boot Option for the parameter 100, the Set Selector and the Block Selector have a specific meaning. Details are given in *System Boot Options Parameter #100* on page 228 for details.

The following table lists which boot properties can be configured and the corresponding boot parameter number.

Table 8-8 Configurable System Boot Option Parameters

Configurable Boot Property	Corresponding Boot Parameter Number
Selection between default and backup boot flash as device to boot from Selection between default and backup EEPROM as device where the on-board FPGA loads its configuration stream from	96

Table 8-8 Configurable System Boot Option Parameters (continued)

Configurable Boot Property	Corresponding Boot Parameter Number
IPMC POST Type	97
Timeout for graceful shutdown	98
BIOS boot parameters as defined in Table 8-15 on page 232	100

8.1.7.1.1 System Boot Options Parameter #96

This boot parameter is an Artesyn-specific OEM boot parameter. Its definition is given in the following table.

Table 8-9 System Boot Options Parameter #96

Data Byte	Description
1	Bits [7:2]: Reserved
	Bit 1: FPGA configuration stream load 0: Load configuration stream from default boot flash 1: Load configuration stream from backup boot flash Note: The new FPGA configuration stream is loaded into the FPGA at the next power-up of the payload.
	Bit 0: Default/backup boot flash selection 0: Boot from default boot flash 1: Boot from backup boot flash Note: The newly selected boot flash is connected to the payload immediately, that means writing to the flash is possible. Its image is executed after the next power-up or cold reset of the payload.

The System Boot Options parameter #96 is non-volatile. During blade production, its data is initialized to 0xFF and its state is set to invalid. Its parameter data remains preserved after IPMC power cycles and firmware upgrades.

8.1.7.1.2 System Boot Options Parameter #97

This boot parameter is an Artesyn-specific OEM parameter. Its definition is given in the following table.

Table 8-10 System Boot Options Parameter #97

Data Byte	Description
1	IPMC POST Type Data 1 - Set Selector. This is the processor ID for which the boot option has to be set.
2	Data 2 - IPMC POST Type Selector. This parameter is used to specify the IPMC POST Type that the IPMC will execute. 0x00: Short POST 0x01: Long POST 0x02 to 0xFF: Not used

The System Boot Options parameter #97 is non-volatile. During blade production, its data is initialized to 0xFF and its state is set to invalid. Its parameter data remains preserved after IPMC power cycles and firmware upgrades.

The System Boot Options parameter #97 is only valid for IPMC.

8.1.7.1.3 System Boot Options Parameter #98

This boot parameter is an Artesyn-specific OEM parameter.

This timer specifies how long the IPMC waits for the payload to shut down gracefully. If the payload software does not configure its OpenIPMI library to be notified for graceful shutdown requests, the IPMC shuts down the payload when the timer expires.

Table 8-11 System Boot Options Parameter #98

Bit	Description
15:8	Timeout for GRACEFUL_SHUTDOWN, LSB (given in 100 msec)
7:0	Timeout for GRACEFUL_SHUTDOWN, MSB (given in 100 msec)

The System Boot Options parameter #98 is non-volatile. During blade production its data is initialized to 0xFF and its state is set to invalid. Its parameter data remains preserved after IPMC power cycles and firmware upgrades.

8.1.7.1.4 System Boot Options Parameter #100

The system boot options parameter #100 allows you to send multiple boot options to the blade's boot firmware and thus control the boot process. The boot options that you can configure using this parameter are typically a subset of the boot options which you can configure in the boot firmware directly, for example, using a setup menu.

The IPMC contains a storage area where the boot parameters are stored. When the blade boots, the boot firmware reads out the storage area, interprets the parameters and executes the boot process accordingly.

The boot parameters in the IPMC storage area have higher priority than the same boot options which may be configured in the firmware itself, for example, using the setup menu.

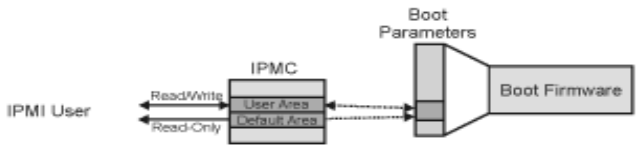
The storage area is divided into two parts: the default area and the user area. The user area can be read and written by an IPMI user and by default is, the area which the boot firmware reads out and uses during the boot process. The default area can only be read by both the IPMI user and the boot firmware. Its purpose is to store factory-programmed default boot options which can be used to restore the standard settings. If you want the boot firmware to read out and use

the boot parameters stored in the default area and thus use the factory settings, you need to configure the blade accordingly. This is typically done by an on-board switch (for example, "Clear CMOS RAM"). It depends on the blade and firmware which settings are stored in the default area. Details are given in the following sections.

On some blades with particular firmware types, changing a boot parameter in the firmware setup menu changes the boot parameter in the user area as well, if the same parameter is defined both in the user area and the set-up menu. Details are given below.

The following figure summarizes the previously explained basic information flow related to the system boot options parameter #100.

Figure 8-1 System Boot Options Parameter #100 - Information Flow Overview



The boot options need to be stored as a sequence of zero terminated strings. The following table describes in detail the format of the boot options to be used when setting or reading the System Boot Options parameter #100.

Table 8-12 System Boot Options - Parameter #100 - Data Format

Byte	Description
0..1	Number of bytes used for boot parameters (LSB first) The number of bytes must be calculated and written into these two bytes by the software which writes into the storage area. The values 0x0000 and 0xFFFF indicate that no data has been written to the storage area. When reading from the storage area and you find any of these two values, your software should assume that no user-specific boot options have previously been written to the storage area.

Table 8-12 System Boot Options - Parameter #100 - Data Format (continued)

Byte	Description
2 .. n	Boot parameters data The boot parameters are stored as ASCII text with the following general format: <name>=<value>, where all name/value pairs are separated by a zero byte. The end of the boot parameter data is indicated by two zero bytes. Allowed and supported name/value pairs are blade-specific. Details are given below.
n + 1 .. n + 2	16 byte checksum over the boot parameters data section. (LSB first) For backward compatibility reasons, the checksums 0x0000 and 0xFFFF are accepted as valid. They indicate that no checksum has been calculated and stored.

When writing to or reading from the storage area, you can only read or write chunks of 16 bytes at a time. For this reason, the default and user area are divided into numbered blocks of 16 bytes which need to be addressed individually. For this purpose, the "Block Selector" field in the request data field is used. The "Set Selector" field, on the other hand, is used to select either the default or user area. The following two tables describe in detail how the request and response data fields need to be filled and interpreted when performing SET and GET accesses.

Table 8-13 System Boot Options Parameter #100 - SET Command Usage

Byte	Description
Request Data	
1	Bit 7: when set to "1", the storage area on the IPMC is locked, i.e. no other software can access it. This should be set, before doing any modifications and cleared again after the final access. Bits [6:0]: must contain the value: "100", indicating this OEM system boot option.
2	Set Selector Must be set to "0" (user area). You can only write to the user area, therefore no other values are supported.
3	Block Selector Zero based index of the 16-byte block which you want to write to. Index 0 refers to the first block of 16 bytes, which includes the first two bytes that indicate the boot parameter data size. Depending on the total length of the boot option data, your software may need to write several blocks of 16 bytes in a row, each individually addressed using the block selector.

Table 8-13 System Boot Options Parameter #100 - SET Command Usage (continued)

Byte	Description
4 .. n (n <= 19)	Data that you want to write into the addressed block. This will be a chunk of the boot parameter data. If less than 16 bytes are written, then only the provided data is written, the remaining bytes in the addressed storage area block are left unchanged.
Response Data	
1	0x00: Write successful 0x80: Boot parameter storage not supported by the IPMC 0x81: Storage area is locked by another software entity 0x82: Illegal write-access 0xC9: Block selector is outside of the allowed range.

Table 8-14 System Boot Options Parameter #100 - GET Command Usage

Byte	Description
Request Data	
1	Bit 7: reserved. Set to "0". Bits [6:0]: must contain the value: "100", indicating this OEM system boot option.
2	Set Selector 0: User area 1: Default area
3	Block Selector Zero based index of the 16-byte block which you want to read from. Index 0 refers to the first block of 16 bytes, which includes the first two bytes which indicate the boot parameter data size.
Response Data	
1	0x00: Read successful 0x80: Boot parameter storage not supported by the IPMC 0xC9: Block selector is outside of the allowed range.
2	Reserved. Set to "1".
3	Bit 7: If set to "1", the addressed storage area is locked. Bits [6:0]: value "100", indicating this OEM boot option command.

Table 8-14 System Boot Options Parameter #100 - GET Command Usage (continued)

Byte	Description
4 .. 19	The content of the read 16-byte block.

In order to detect the maximum size of writable storage area, your software can perform a series of read accesses while incrementing the block selector with each access. Once the error code C9 is returned, the limit has been reached and the total available space in the writable storage area can be easily determined by the number of previously performed successful read accesses.

This is supported by HPI, for details refer to the *System Management Interface Based on HPI-B User's Guide* related to your system environment.

The following table lists boot parameters which can be configured for the ATCA-7365-CE blade, using the system boot option parameter #100.

Artesyn Embedded Technologies provides the tool "ipmibpar" to interpret the ASCII parameters. To obtain the tool, contact your local sales representative.

When used in the System Boot Options parameter #100, the boot parameters and their values are case-sensitive.

All boot options listed in the following table are set by the BIOS setup menu and can be configured using the System Boot options command #100. The IPMC and BIOS software automatically synchronize the settings made in the BIOS setup menu and the settings specified using the System Boot Options command #100. Changing a parameter in either of these, automatically changes the respective value in the other.

Table 8-15 System Boot Options Parameter #100 - Supported Parameters

Parameter	Description	Values
baudrate	Console baud rate	9600/19200/57600/115200
usb	USB support	fp_on/fp_off,rtm_on/rtm_off,onboard_on/onboard_off Example: usb=fp_off, rtm_off, onboard_on -> Front panel USB off, RTM USB off, Onboard Flash USB on

Table 8-15 System Boot Options Parameter #100 - Supported Parameters (continued)

Parameter	Description	Values
os_boot_watchdog	OS boot Watchdog (IPMI)	on/off, timeout in minutes, action Timeout range 1,2,3,5,7,10,15,20 action: no action/reset/power off/power cycle Example: os_boot_watchdog=on,10,reset -> watchdog is on, 10 minutes timeout, action=reset
rtm_auto	Auto detect RTM If enabled (on), the parameter for 'Force Gen1' and RTM PCIe configuration is set correctly.	on/off: auto detect on/off gen1on/gen1off: Force Gen1 on/off x4x4x4x4/x4x4x8/x8x4x4/x8x8/x16: PCIe bifurcation Example: rtm_auto=off,gen1on,x4x4x8 -> RTM auto detect off, Force Gen1 on, PCIe x4x4x8
frontnet_boot	Boot from Front Panel Network	off/on
basenet_boot	Boot from Base Network	off/on
artm_net_boot	Boot from ARTM Network	off/on
artm_sas_boot	Boot from ARTM SAS device	off/on
artm_fc_boot	Boot from ARTM FC device	off/on
boot_order	Boot priority order	device1,devcice2,..device8 See *boot_order Devices*
uefi#	UEFI Media path	Format: NAME=DevicePath This parameter contains a UEFI Device path in text form. This parameter is saved at boot time. The Installer from a UEFI compatible OS writes this parameter to NVRAM and after the next reboot BIOS stores this to IPMI boot parameter

Table 8-16 boot_order Devices

Device	Description
sata0	SATA device 0 (Debug SATA)

Table 8-16 boot_order Devices (continued)

Device	Description
sata1	SATA device 1 (RTM Debug SATA)
sata5	SATA device 5 (Onboard SATA)
sataonboard	SATA device 5 (Onboard SATA)
sashdd	SAS HDD mounted on the RTM
sas0_nn	SAS Controller nn = SCSI ID (use this when a SAS array is connected to the RTM)
frontnet	Front Panel Network
basenet0	Base Ethernet Interface Channel 1
basenet1	Base Ethernet Interface Channel 2
fabricnet0	Fabric Ethernet Interface Channel 1
fabricnet1	Fabric Ethernet Interface Channel 2
usb1	USB frontpanel 1
usb2	USB frontpanel 2
usbonboard	USB onboard HDD
usbartm	USB artm
usbkey	USB key
usbcdrom	USB cdrom
usbhdd	USB hdd
usbfdd	USB floppy disk
efishell	Built in UEFI shell
uefi#	UEFI Media path place holder which points to the corresponding uefi# parameter
Up to 10 boot devices are supported. Example: boot_order=sas0_03,basenet0,usbkey,sata1 Note: uefi network devices are only available when Network Stack in Advanced Setup Menu is set to enabled.	

8.1.8 LAN Device Commands

The following table provides the LAN Device Commands information.

Table 8-17 Supported LAN Device Commands

Command	NetFn (Request/Response)	CMD
Set LAN Configuration Parameters	0x0C/0x0D	0x01
Get LAN Configuration Parameters	0x0C/0x0D	0x02
Set SOL Configuration Parameters	0x0C/0x0D	0x21
Get SOL Configuration Parameters	0x0C/0x0D	0x22

8.2 PICMG 3.0 Commands

The Artesyn Embedded Technologies IPMC is a fully compliant AdvancedTCA intelligent Platform Management Controller. It supports all required and mandatory AdvancedTCA commands as defined in the PICMG 3.0 and AMC.0 R2.0 specifications.

Table 8-18 Supported PICMG 3.0 Commands

Command	NetFn (Request/Response)	CMD	Comments
Get PICMG Properties	0x2C/0x2D	0x00	-
Get Address Info	0x2C/0x2D	0x01	-
FRU Control	0x2C/0x2D	0x04	The blade supports the cold reset and graceful reboot options.
Get FRU LED Properties	0x2C/0x2D	0x05	-
Get FRU LED Color Capabilities	0x2C/0x2D	0x06	-
Set FRU LED State	0x2C/0x2D	0x07	-
Get FRU LED State	0x2C/0x2D	0x08	-
Set IPMB State	0x2C/0x2D	0x09	-
Set FRU Activation Policy	0x2C/0x2D	0x0A	-
Get FRU Activation Policy	0x2C/0x2D	0x0B	-

Table 8-18 Supported PICMG 3.0 Commands (continued)

Command	NetFn (Request/Response)	CMD	Comments
Set FRU Activation	0x2C/0x2D	0x0C	-
Get Device Locator Record ID	0x2C/0x2D	0x0D	The Artesyn Embedded Technologies IPMCs support the standard PICMG 3.0 and the extended AMC.0 R2.0 versions of this command.
Set Port State	0x2C/0x2D	0x0E	-
Get Port State	0x2C/0x2D	0x0F	-
Compute Power Properties	0x2C/0x2D	0x10	-
Set Power Level	0x2C/0x2D	0x11	-
Get Power Level	0x2C/0x2D	0x12	-
Get IPMB Link Info	0x2C/0x2D	0x18	-
Set AMC Port State	0x2C/0x2D	0x19	-
Get AMC Port State	0x2C/0x2D	0x1A	-
Get FRU Control Capabilities	0x2C/0x2D	0x1E	-
Get target upgrade capabilities	0x2C/0x2D	0x2E	-
Get component properties	0x2C/0x2D	0x2F	-
Abort firmware upgrade	0x2C/0x2D	0x30	-
Initiate upgrade action	0x2C/0x2D	0x31	-
Upload firmware block	0x2C/0x2D	0x32	-
Finish firmware upload	0x2C/0x2D	0x33	-
Get upgrade status	0x2C/0x2D	0x34	-
Activate firmware	0x2C/0x2D	0x35	-
Query self-test results	0x2C/0x2D	0x36	-
Query rollback status	0x2C/0x2D	0x37	-
Initiate manual rollback	0x2C/0x2D	0x38	-

The firmware upgrade commands supported by the blade are implemented according to the PICMG HPM.1 Revision 1.0 specification.

The boot block can be updated with PICMG HPM.1 specific commands.

8.2.1 Set/Get Power Level

The blade supports two power levels. In case of a shelf which only allows 200W per slot the P-States of the blade will be restricted to match this requirement. The second power level has no restrictions.

For more information, refer to Chapter 4, *BIOS, on page 87*.

8.3 Artesyn Specific Commands

The Artesyn IPMC supports several commands which are not defined in the IPMI or PICMG 3.0 specification but are introduced by Artesyn serial output commands.

- Before sending any of these commands, the shelf management software must check whether the receiving IPMI controller supports Artesyn specific IPMI commands by using the IPMI command 'Get Device ID'. Sending Artesyn specific commands to IPMI controllers which do not support these IPMI commands will lead to no or undefined results.
- Proper handling of these commands is required to write a portable application.

8.3.1 Serial Output Commands

The following table provides the LAN Device Commands information.

Table 8-19 Serial Output Commands

Command Name	NetFn (Request/Response)	CMD	Description
Set Serial Output	0x2E/0x2F	0x15	See *Set Serial Output Command* on page 238
Get Serial Output	0x2E/0x2F	0x16	See *Get Serial Output Command* on page 239

8.3.1.1 Set Serial Output Command

The Set Serial Output command selects the serial port output source for a serial port connector.

8.3.1.1.1 Request Data

The following table lists the request data applicable to the Set Serial Output command.

Table 8-20 Request Data of Set Serial Output Command

Byte	Data Field
1	LSB of Artesyn Embedded Technologies IANA Enterprise number. A value of 0xCD has to be used.
2	Second byte of Artesyn Embedded Technologies IANA Enterprise number. A value of 0x65 has to be used.
3	MSB of Artesyn Embedded Technologies IANA Enterprise number. A value of 0x00 has to be used.
4	Serial connector type 0: Faceplate connector 1: Backplane connector All other values are reserved. Note: Only the faceplate connector is supported. No connector on the RTM available.
5	Serial connector instance number. A sequential number that starts from "0".

Table 8-20 Request Data of Set Serial Output Command (continued)

Byte	Data Field
6	Serial output selector 0: BIOS 2: IPMC debug console All other values are reserved.

8.3.1.1.2 Response Data

The following table lists the response data applicable to the Set Serial Output command.

Table 8-21 Response Data of Set Serial Output Command

Byte	Data Field
1	Completion code
2	LSB of Artesyn IANA Enterprise number.
3	Second byte of Artesyn IANA Enterprise number.
4	MSB of Artesyn IANA Enterprise number.

8.3.1.2 Get Serial Output Command

The Get Serial Output Command provides a way to determine which serial output source goes to a particular serial port connector.

Currently, only BIOS output is supported.

8.3.1.2.1 Request Data

The following table lists the request data applicable to the Get Serial Output command.

Table 8-22 Request Data of Get Serial Output Command

Byte	Data Field
1	LSB of Artesyn IANA Enterprise number. A value of 0xCD has to be used.
2	Second byte of Artesyn IANA Enterprise number. A value of 0x65 has to be used.
3	MSB of Artesyn IANA Enterprise number. A value of 0x00 has to be used.
4	Serial connector type 0: Faceplate connector 1: Backplane connector All other values are reserved. Note: Only the faceplate connector is supported. No connector on the RTM available.
5	Serial connector instance number. A sequential number that starts from 0.

8.3.1.2.2 Response Data

The following table lists the response data applicable to the Get Serial Output command.

Table 8-23 Response Data of Get Serial Output Command

Byte	Data Field
1	Completion code
2	LSB of Artesyn IANA Enterprise number.
3	Second byte of Artesyn IANA Enterprise number.
4	MSB of Artesyn IANA Enterprise number.
5	Serial output selector

8.4 Pigeon Point Specific Commands

The IPMC supports additional IPMI commands that are specific to Pigeon Point. This section provides detailed descriptions of those extensions.

Table 8-24 Pigeon Point Extension Commands

Command	NetFn (Request/Response)	CMD
Get Status Table 8-26 on page 242	0x2E/0x2F	0x00
Get Serial Interface Properties Table 8-27 on page 245	0x2E/0x2F	0x01
Set Serial Interface Properties Table 8-28 on page 246	0x2E/0x2F	0x02
Get Debug Level Table 8-29 on page 247	0x2E/0x2F	0x03
Set Debug Level Table 8-30 on page 248	0x2E/0x2F	0x04
Get Hardware Address Table 8-31 on page 249	0x2E/0x2F	0x05
Set Hardware Address Table 8-32 on page 249	0x2E/0x2F	0x06
Get Handle Switch Table 8-33 on page 250	0x2E/0x2F	0x07
Set Handle Switch Table 8-34 on page 251	0x2E/0x2F	0x08
Get Payload Communication Time-Out Table 8-35 on page 251	0x2E/0x2F	0x09
Set Payload Communication Time-Out Table 8-36 on page 252	0x2E/0x2F	0x0A
Enable Payload Control Table 8-37 on page 253	0x2E/0x2F	0x0B
Disable Payload Control Table 8-38 on page 253	0x2E/0x2F	0x0C
Reset IPMC Table 8-39 on page 254	0x2E/0x2F	0x0D
Hang IPMC Table 8-40 on page 254	0x2E/0x2F	0x0E
Graceful Reset Table 8-41 on page 255	0x2E/0x2F	0x11
Get Payload Shutdown Time-Out Table 8-42 on page 256	0x2E/0x2F	0x15
Set Payload Shutdown Time-Out Table 8-43 on page 257	0x2E/0x2F	0x16
Get Module State Table 8-44 on page 257	0x2E/0x2F	0x27
Enable Module Site Table 8-45 on page 259	0x2E/0x2F	0x28
Disable Module Site Table 8-46 on page 259	0x2E/0x2F	0x29

Table 8-24 Pigeon Point Extension Commands (continued)

Command	NetFn (Request/Response)	CMD
Reset Carrier SDR repository Table 8-47 on page 260	0x2E/0x2F	0x33

Some of the following commands refer to IPMC modes which are defined as following table

Table 8-25 IPMC Modes

Mode	Description
Standalone	In standalone mode, the carrier IPMC disconnects from IPMB-0 but keeps on listening to the serial debug and payload interfaces and serving requests coming from them, as well as managing the modules, AMC point-to-point (P2P) and clock E-keying. Standalone mode is intended for debugging purposes and/or operation in a non-ATCA environment. In standalone mode, the carrier IPMC automatically activates and deactivates the on-carrier payload and modules whenever it does not violate any carrier limitations.
Manual standalone	Manual standalone mode is equivalent to standalone mode with only one exception: carrier IPMC control over the on-carrier payload is automatically disabled in manual standalone mode.

8.4.1 Get Status Command

The Get Status command can be used by the payload software to retrieve the status of the IPMC.

Table 8-26 Get Status Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

Table 8-26 Get Status Command Description (continued)

Type	Byte	Data Field
	5	Bit [7] Graceful Reboot Request If set to 1, indicates that the payload is requested to initiate the graceful reboot sequence. Bit [6] Diagnostic Interrupt Request If set to 1, indicates that a payload diagnostic interrupt request has arrived. Bit [5] Shutdown Alert If set to 1, indicates that the payload is going to be shutdown. Bit [4] Reset Alert If set to 1, indicates that the payload is going to be reset. Bit [3] Sensor Alert If set to 1, indicates that at least one of the IPMC sensors detects a threshold crossing. Bits [2:1] Mode The current IPMC modes are defined as: 0: Normal 1: Standalone, for a description refer to Table 8-25 2: Manual Standalone, for a description refer to Table 8-25 Bit [0] Control If set to 0, the IPMC control over the payload is disabled.
	6	Bits [4:7] Metallic Bus 2 Events These bits indicate pending Metallic Bus 2 requests arrived from the shelf manager: 0: Metallic Bus 2 Query 1: Metallic Bus 2 Release 2: Metallic Bus 2 Force 3: Metallic Bus 2 Free Bits [0:3] Metallic Bus 1 Events These bits indicate pending Metallic Bus 1 requests arrived from the shelf manager: 0: Metallic Bus 1 Query 1: Metallic Bus 1 Release 2: Metallic Bus 1 Force 3: Metallic Bus 1 Free

Table 8-26 Get Status Command Description (continued)

Type	Byte	Data Field
	7	Bits [4:7] Clock Bus 2 Events These bits indicate pending Clock Bus 2 requests arrived from the shelf manager: 0: Clock Bus 2 Query 1: Clock Bus 2 Release 2: Clock Bus 2 Force 3: Clock Bus 2 Free Bits [0:3] Clock Bus 1 Events These bits indicate pending Clock Bus 1 requests arrived from the shelf manager: 0: Clock Bus 1 Query 1: Clock Bus 1 Release 2: Clock Bus 1 Force 3: Clock Bus 1 Free
	8	Bits [4:7] Reserved Bits [0:3] Clock Bus 3 Events These bits indicate pending Clock Bus 3 requests arrived from the shelf manager: 0: Clock Bus 3 Query 1: Clock Bus 3 Release 2: Clock Bus 3 Force 3: Clock Bus 3 Free

8.4.2 Get Serial Interface Properties Command

The Get Serial Interface Properties command is used to get the properties of a particular serial interface.

Table 8-27 Get Serial Interface Properties Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Interface ID 0: Serial Debug Interface
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00
	5	Bit [7] Echo On If this bit is set, the IPMC enables echo for the given serial interface. Bits [6:4] Reserved Bits [3:0] Baud Rate ID The baud rate ID defines the interface baud rate as follows: 0: 9600 bps 1: 19200 bps 2: 38400 bps 3: 57600 bps (unsupported) 4: 115200 bps (unsupported)

8.4.3 Set Serial Interface Properties Command

The Set Serial Interface Properties command is used to set the properties of a particular serial interface.

Table 8-28 Set Serial Interface Properties Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Interface ID 0: Serial Debug Interface
	5	Bit [7] Echo On If this bit is set, the IPMC enables echo for the given serial interface. Bits [6:4] Reserved Bits [3:0] Baud Rate ID The baud rate ID defines the interface baud rate as follows: 0: 9600 bps 1: 19200 bps 2: 38400 bps 3: 57600 bps (unsupported) 4: 115200 bps (unsupported)
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.4 Get Debug Level Command

The Get Debug Level command gets the current debug level of the IPMC firmware.

Table 8-29 Get Debug Level Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00
	5	Bit [7] IPMB-L Dump Enable If set to "1", the IPMC provides a trace of IPMB-L messages that are arriving to/going from the IPMC via IPMB-L. Bit [6] n/a Bit [5] KCS Dump Enable If set to "1", the IPMC provides a trace of KCS messages that are arriving to/going from the IPMC via KCS. Bit [4] IPMB Dump Enable If set to "1", the IPMC provides a trace of IPMB messages that are arriving to/going from the IPMC via IPMB-O. Bit [3] n/a Bit [2] Alert Logging Enable If set to "1", the IPMC outputs important alert messages onto the serial debug interface. Bit [1] Low-level Error Logging Enable If set to "1", the IPMC outputs low-level error/diagnostic messages onto the serial debug interface. Bit [0] Error Logging Enable If set to "1", the IPMC outputs error/diagnostic messages onto the serial debug interface.

8.4.5 Set Debug Level Command

The Set Debug Level command sets the current debug level of the IPMC firmware.

Table 8-30 Set Debug Level Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Bit [7] IPMB-L Dump Enable If set to "1", the IPMC provides a trace of IPMB-L messages that are arriving to/going from the IPMC via IPMB-L. Bit [6] n/a Bit [5] KCS Dump Enable If set to "1", the IPMC provides a trace of KCS messages that are arriving to/going from the IPMC via KCS. Bit [4] IPMB Dump Enable If set to "1", the IPMC provides a trace of IPMB messages that are arriving to/going from the IPMC via IPMB-O. Bit [3] n/a Bit [2] Alert Logging Enable If set to "1", the IPMC outputs important alert messages onto the serial debug interface. Bit [1] Low-level Error Logging Enable If set to "1", the IPMC outputs low-level error/diagnostic messages onto the serial debug interface. Bit [0] Error Logging Enable If set to "1", the IPMC outputs error/diagnostic messages onto the serial debug interface.
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.6 Get Hardware Address Command

The Get Hardware Address command reads the hardware address of the IPMC.

Table 8-31 Get Hardware Address Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00
	5	Hardware Address

8.4.7 Set Hardware Address Command

The Set Hardware Address command allows to override the hardware address read from hardware when the IPMC operates in (manual) standalone mode (for description refer to Table 8-25).

Table 8-32 Set Hardware Address Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Hardware Address If set to 00, the ability to override the hardware address is disabled. Note: A hardware address change only takes effect after an IPMC reset.
Response Data	1	Completion Code

Table 8-32 Set Hardware Address Command Description (continued)

Type	Byte	Data Field
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.8 Get Handle Switch Command

The Get Handle Switch command reads the state of the hot-swap handle of the IPMC. Overriding of the handle switch state is allowed only if the IPMC operates in manual standalone mode (for description refer to Table 8-25).

Table 8-33 Get Handle Switch Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	FRU ID (specify as 0)
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00
	5	Handle Switch Status 0x00: The handle switch is open. 0x01: The handle switch is closed. 0x02: The handle switch state is read from hardware.

8.4.9 Set Handle Switch Command

The Set Handle Switch command sets the state of the hot-swap handle switch in manual standalone mode (for description refer to Table 8-25).

Table 8-34 Set Handle Switch Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	FRU ID (specify as 0)
	5	Handle Switch Status 0x00: The handle switch is open. 0x01: The handle switch is closed. 0x02: The handle switch state is read from hardware.
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.10 Get Payload Communication Time-Out Command

The Get Payload Communication Time-Out command reads the payload communication time-out value.

Table 8-35 Get Payload Communication Time-Out Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code

Table 8-35 Get Payload Communication Time-Out Command Description (continued)

Type	Byte	Data Field
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00
	5	Payload Time-out Payload communication time-out measured in hundreds of milliseconds. Thus, the payload communication time-out may vary from 0.1 to 25.5 seconds.

8.4.11 Set Payload Communication Time-Out Command

The Set Payload Communication Time-Out command sets the payload communication time-out value.

Table 8-36 Set Payload Communication Time-Out Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Payload Time-out Payload communication time-out measured in hundreds of milliseconds. Thus, the payload communication time-out may vary from 0.1 to 25.5 seconds.
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.12 Enable Payload Control Command

The Enable Payload Control command enables payload control from the serial debug interface.

Table 8-37 Enable Payload Control Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.13 Disable Payload Control Command

The Disable Payload Control command disables payload control from the serial debug interface.

Table 8-38 Disable Payload Control Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.14 Reset IPMC Command

The Reset IPMC command allows the payload to reset the IPMC over the KCS host interface.

Table 8-39 Reset IPMC Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Reset Type Code 0x00: Cold IPMC reset to the current mode 0x01: Cold IPMC reset to the Normal mode 0x02: Cold IPMC reset to the Standalone mode, for more details refer to Table 8-25. 0x03: Cold IPMC reset to the Manual Standalone mode, for more details refer to Table 8-25. 0x04: Reset the IPMC and enter Upgrade mode
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.15 Hang IPMC Command

The IPMC provides a way to test the watchdog timer support by implementing the Hang IPMC command, which simulates firmware hanging by entering an endless loop.

Table 8-40 Hang IPMC Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code

Table 8-40 Hang IPMC Command Description (continued)

Type	Byte	Data Field
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.16 Graceful Reset Command

The IPMC supports the Graceful Reboot option of the FRU Control command. On receiving such a command, the IPMC sets the Graceful Reboot Request bit of the IPMC status, sends a status update notification to the payload, and waits for the Graceful Reset command from the payload. If the IPMC receives such a command before the payload communication time-out time, it sends the 0x00 completion code (Success) to the shelf manager. Otherwise, the 0xCC completion code is sent.

The IPMC does not reset the payload upon receiving the Graceful Reset command or time-out. If the IPMC participation is necessary, the payload must request the IPMC to perform a payload reset. The Graceful Reset command is also used to notify the IPMC about the completion of the payload shutdown sequence.

Table 8-41 Graceful Reset Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.17 Get Payload Shutdown Time-Out Command

When the shelf manager commands the IPMC to shut down the payload (i.e. sends the Activate FRU (Deactivate) command), the IPMC notifies the payload by forwarding the command Activate FRU (Deactivate) to the KCS interface. Provided the OpenIPMI driver has registered this command for notification, the payload gets notified. Upon receiving this notification, the payload software is expected to initiate the payload shutdown sequence. After performing this sequence, the payload should send the Graceful Reset command to the IPMC over the payload Interface to notify the IPMC that the payload shutdown is complete.

To avoid deadlocks that may occur if the payload software does not respond, the IPMC provides a special time-out for the payload shutdown sequence. If the payload does not send the Graceful Reset command within a definite period of time, the IPMC assumes that the payload shutdown sequence is finished, and resets the payload.

Table 8-42 Get Payload Shutdown Time-Out Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00
	5:6	Time-Out measured in hundreds of milliseconds, LSB first

8.4.18 Set Payload Shutdown Time-Out Command

The Set Payload Shutdown Time-Out command is defined as follows.

Table 8-43 Set Payload Shutdown Time-Out Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4:5	Time-Out measured in hundreds of milliseconds, LSB first
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.19 Get Module State Command

The Get Module State command is used to query the state of a module (RTM with site ID1) using any of the external interfaces.

Table 8-44 Get Module State Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Module Site ID
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

Table 8-44 Get Module State Command Description (continued)

Type	Byte	Data Field
	5	Module Status Bit [0] 0: Module site is enabled. 1: Module site is disabled. Bit [1] 0: Module is not present. 1: Module is present. Bit [2] 0: Management power is disabled. 1: Management power is enabled. Bit [3] 0: Management power is bad. 1: Management power is good. Bit [4] 0: Payload power is disabled. 1: Payload power is enabled. Bit [5] 0: Payload power is bad. 1: Payload power is good. Bit [6] 0: IPMB-L buffer is not attached. 1: IPMB-L buffer is attached. Bit [7] 0: IPMB-L buffer is not ready. 1: IPMB-L buffer is ready.

8.4.20 Enable Module Site Command

The Enable Module Site command is used to enable a module site.

Table 8-45 Enable Module Site Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Module Site ID
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00

8.4.21 Disable Module Site Command

The Disable Module Site command is used to disable a module site. If a module site is disabled, the IPMC firmware ignores the module inserted and acts as if the module is not present.

Table 8-46 Disable Module Site Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Module Site ID
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.22 Reset Carrier SDR Repository Command

The Reset Carrier SDR Repository command is used to clear and rebuild the carrier SDR repository.

Table 8-47 Reset Carrier SDR Repository Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

9.1 FRU Information

The blade provides the following FRU information in FRU ID 0.

Table 9-1 FRU Information

Area	Description	Value	Access
Internal use area	Not used		
Board info area	Mfg date / time	According to Platform Management FRU information Storage Definition v1.0	r
	Board manufacturer	'ARTESYN'	r
	Board product name	Product name of the specific blade variant	r
	Board serial number	Defined by Artesyn Embedded Technologies	r
	Board part number	Defined by Artesyn Embedded Technologies	r
Product info area	Product manufacturer	'ARTESYN'	r
	Product name	Product name of the specific blade variant	r
	Product serial number	Defined by Artesyn Embedded Technologies	r
	Product part number	Defined by Artesyn Embedded Technologies	r
Multi record info area	Blade Point-To-Point Connectivity Record Area	This multi record area contains the ATCA-blade Point to Point Connectivity Record according to PICMG 3.0, Rev.1.0. The contents are described in the section 'E-Keying'.	r
	User Info Area	Artesyn OEM ID: 0x48, 0x0E, 0x00, 0x00 Followed by 255 byte of user info area data	r/w
	Custom usage	Minimum 256 Byte available	r/w

9.2 MAC Address Record

The blade provides one OEM FRU record which contains information about on-board MAC addresses.

The format of the record is described in the following table.

Table 9-2 Artesyn MAC Addresses Record

Offset	Length	Description
0	1	Record Type ID. A value of C0h (OEM) shall be used for Artesyn OEM records.
1	1	End of List / Version [7] End of List. Set to 1b for the last record [6:4] Reserved. Write as 000b. [3:0] Record format version. Write as 2h.
2	1	Record Length
3	1	Record Checksum (zero checksum)
4	1	Header Checksum (zero checksum)
5	1	LSB of Manufacturer ID. Write as CDh.
6	1	Second Byte of Manufacturer ID. Write as 65h.
7	1	MSB of Manufacturer ID. Write as 00h.
8	1	Artesyn Record ID. 01h for Artesyn MAC Address Record.
9	1	Record Format Version. 00h for this specification.
10	1	Number of MAC Address Descriptors (N).
11	N*7	Artesyn MAC Address Descriptors. Refer Table "Artesyn MAC Address Descriptor" on page 262 for details of Artesyn MAC Address Descriptor.

Table 9-3 Artesyn MAC Address Descriptor

Offset	Length	Description
0	1	Interface Type. Refer to the table below for Interface Type Assignments.
1	6	MAC Address. First Octet comes first.

Table 9-4 Interface Type Assignments

Interface Type	Description
01h	ATCA Base Interface or AMC / MicroTCA Common Options Region
02h	ATCA Fabric Interface or AMC / MicroTCA Fat Pipe Region
03h	Front Panel
04h	AMC / MicroTCA Extended Fat Pipe Region

9.3 E-Keying

The following table lists the e-keying information provided by the blade. The respective information is contained in the point-to-point connectivity record area.

The fibre channel interfaces (link type extension 2) described in the point-to-point connectivity record area are physically not supported by the blade.

The following table details the contents of the Blade Point-to-Point Connectivity Record Area.

Table 9-5 Contents of the Blade Point-to-Point Connectivity Record Area

No.	Link Grouping ID	Interface	Channel Number	Ports	Link Type	Link Type Extension	Link Descriptor Value
1	0	0 (Base Interface)	1	0 -SET 1 - NOT SET 2 - NOT SET 3 - NOT SET	0x01	0	
2	0	0 (Base Interface)	2	0 -SET 1 - NOT SET 2 - NOT SET 3 - NOT SET	0x01	1	
3	0	1 (Fabric Interface)	1	0 -SET 1 - SET 2 -SET 3 -SET	0x02	1	
4	0	1 (Fabric Interface)	1	0 -SET 1 - NOT SET 2 - NOT SET 3 - NOT SET	0x02	0	
5	0	1 (Fabric Interface)	2	0 -SET 1 - SET 2 -SET 3 -SET	0x02	1	
6	0	1 (Fabric Interface)	2	0 -SET 1 - NOT SET 2 - NOT SET 3 - NOT SET	0x02	0	
7	0	2 (Update Channel Interface)	1	0 -SET 1 - NOT SET 2 - NOT SET 3 - NOT SET	0xF0	0	

Table 9-5 Contents of the Blade Point-to-Point Connectivity Record Area (continued)

No.	Link Grouping ID	Interface	Channel Number	Ports	Link Type	Link Type Extension	Link Descriptor Value
8	0	2 (Update Channel Interface)	2	0 -SET 1 - NOT SET 2 - NOT SET 3 - NOT SET	0xF1	0	
9	0	2 (Update Channel Interface)	2	0 - NOT SET 1 - SET 2 - NOT SET 3 - NOT SET	0xF2	0	
10	0	2 (Update Channel Interface)	2	0 - NOT SET 1 - NOT SET 2 - SET 3 - NOT SET	0xF3	0	
11	0	2 (Update Channel Interface)	2	0 - NOT SET 1 - NOT SET 2 - NOT SET 3 - SET	0xF4	0	

9.4 Power Configuration

The following table provides the power configuration information.

Table 9-6 Power Configuration

Item	Value	Description
Dynamic power reconfiguration support	No	While the blade is powered, it supports only one power level.
Dynamic power configuration	No	The power level is fixed and does not change).
Number of power draw levels	2	The amount of possible power levels
Early Power Draw Levels, Watt	-	Complete early power level including IPMC
Steady state Power Draw Levels, Watt	2.0 GHz 6x4GB DDR3 + RTM = 180 - 220 Watts Max - 260 Watts	Complete steady power consumption including IPMC
Transition from early to steady levels, sec	0s	-

9.5 Sensor Data Records

The sensors available on the blades are shown in the table below. See Table 9-8 on page 270 for a detailed description of the Sensor Data Records.

Table 9-7 IPMI Sensors Overview

Sensor Name	Sensor Type	Sensor Number
1.2V	Voltage	0x0A
1.5V	Voltage	0x09
1.5V DDR3	Voltage	0x0C
1.8V Eth	Voltage	0x08
12.0V	Voltage	0x05

Table 9-7 IPMI Sensors Overview (continued)

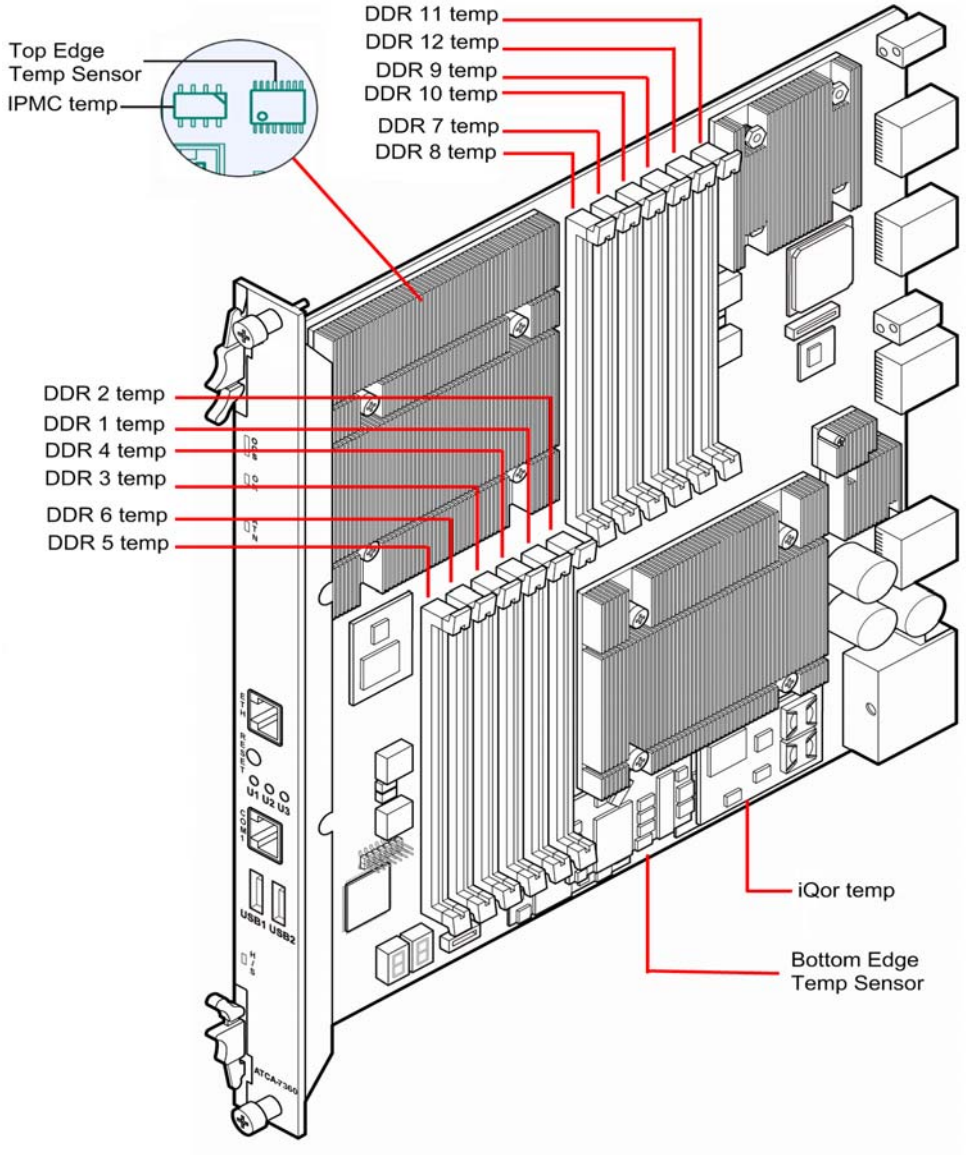
Sensor Name	Sensor Type	Sensor Number
3.3V	Voltage	0x06
3.3V Mgmt	Voltage	0x07
-48v Amps	Current	0x2B
-48v A Volts	Voltage	0x29
-48v B Volts	Voltage	0x2A
ATCA-7360 IPMC	Artesyn IPMC Status	0x15
BMC Watchdog	Watchdog 2	0x04
Boot Bank	Artesyn-specific Discrete Digital	0x10
Boot Error	Boot Error	0x13
Boot Initiated	System Boot Initiated	0x14
CPU0 temp	Temperature	0x27
CPU1 temp	Temperature	0x28
CPU Status	Processor	0x26
DDR 1 temp	Temperature	0x19
DDR 2 temp	Temperature	0x1A
DDR 3 temp	Temperature	0x1B
DDR 4 temp	Temperature	0x1C
DDR 5 temp	Temperature	0x1D
DDR 6 temp	Temperature	0x1E
DDR 7 temp	Temperature	0x1F
DDR 8 temp	Temperature	0x20
DDR 9 temp	Temperature	0x21
DDR 10 temp	Temperature	0x22
DDR 11 temp	Temperature	0x23
DDR 12 temp	Temperature	0x24
Fw Progress	System Firmware Progress	0x11

Table 9-7 IPMI Sensors Overview (continued)

Sensor Name	Sensor Type	Sensor Number
HoldUp Cap Volts	Voltage	0x2C
Hot Swap Carrier	PICMG 3.0: FRU HotSwap	0x00
Hotswap_RTM Sensor	PICMG 3.0: FRU HotSwap	0x01
Bottom Edge Temp Sensor	Temperature	0x0D
IPMB Physical	PICMG 3.0: IPMB Physical Link	0x03
IPMC POST	Management Subsystem Health	0x0F
IPMC temp	Temperature	0x25
OS Boot	OS Boot	0x12
Top Edge Temp Sensor	Temperature	0x0E
POST code	Artesyn-specific Discrete Digital	0x17
PWR Entry Temp	Temperature	0x2D
PWR Entry Status	OEM reserved	0x2E
Power Good	Entity Presence	0x16
Reset Source	Artesyn-specific Discrete Digital	0x18
VCC CPU0	Voltage	0x0B
Version change	Version Change	0x02

The following figure shows the locations of all temperature sensors available on board.

Figure 9-1 Location of Temperature Sensors



The sensors available on the blades are detailed in the table below.

For sensor threshold definition please use the "ipmitool" found on http://sourceforge.net/projects/ipmitool/files/ipmitool/ with the parameter "sensor".

Table 9-8 Sensor Data Records

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/Description	Assertion Deassertion	Rearm
0	Hot Swap Carrier	Hot Swap 0xF0	Sensor-specific discrete 0x6F	0x0 0x1 0x2 0x3 0x4 0x5 0x6 0x7	[7:4] = Cause [3:0] = Previous State	FRU ID	0x0: M0 0x1: M1 0x2: M2 0x3: M3 0x4: M4 0x5: M5 0x6: M6 0x7: M7	Asrt	Auto
1	Hotswap_RTM	Hot Swap 0xF0	Sensor-specific discrete 0x6F	0x0 0x1 0x2 0x3 0x4 0x5 0x6 0x7	[7:4] = Cause [3:0] = Previous State	FRU ID	0x0: M0 0x1: M1 0x2: M2 0x3: M3 0x4: M4 0x5: M5 0x6: M6 0x7: M7	Asrt	Auto
2	Version change	Version Change 0x2B	Sensor-specific discrete 0x6F	0x7	Change type	0xFF	0x7: Software or F/W change successful	Asrt	Auto
3	IPMB Physical	Physical IPMB-0 0xF1	Sensor-specific discrete 0x6F	0x0 0x1 0x2 0x3	[7:4] = Channel Number [3:0] = Reserved	reading	0x0: IPMB-A disabled, IPMB-B disabled 0x1: IPMB-A enabled, IPMB-B disabled 0x2: IPMB-A disabled, IPMB-B enabled 0x3: IPMB-A enabled, IPMB-B enabled	Asrt	Auto

Asrt: Assertion
Deass: Deassertion
Unr: Upper non-recoverable threshold
Lnr: Lower non-recoverable threshold
Uc: Upper critical threshold
Lc: Lower critical threshold
Unc: Upper non-critical threshold
Lnc: Lower non-critical threshold

Table 9-8 Sensor Data Records (continued)

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/Description	Assertion Deassertion	Rearm
4	BMC Watchdog	Watchdog 2 0x23	Sensor-specific discrete 0x6F	0x0 0x1 0x2 0x3 0x8	See IPMI Spec	0xFF	0x0: Timer expired 0x1: Hard Reset 0x2: Power Down 0x3: Power Cycle 0x8: Timer Interrupt	Asrt	Auto
5	12.0V	Voltage 0x02	Threshold 0x01		reading	threshold	unr uc lnr lc	Asrt / Deass	Auto
6	3.3V	Voltage 0x02	Threshold 0x01		reading	threshold	unr uc lnr lc	Asrt / Deass	Auto
7	3.3V Mgmt	Voltage 0x02	Threshold 0x01		reading	threshold	unr uc lnr lc	Asrt / Deass	Auto
8	1.8V Eth	Voltage 0x02	Threshold 0x01		reading	threshold	unr uc lnr lc	Asrt / Deass	Auto
9	1.5V	Voltage 0x02	Threshold 0x01		reading	threshold	unr uc lnr lc	Asrt / Deass	Auto
10	1.2V	Voltage 0x02	Threshold 0x01		reading	threshold	unr uc lnr lc	Asrt / Deass	Auto
11	VCC CPU0	Voltage 0x02	Threshold 0x01		reading	threshold	unr uc lnr lc	Asrt / Deass	Auto
12	1.5V DDR3	Voltage 0x02	Threshold 0x01		reading	threshold	unr uc lnr lc	Asrt / Deass	Auto
13	Bottom Edge Temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
14	Top Edge Temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto

Asrt: Assertion
Deass: Deassertion
Unr: Upper non-recoverable threshold
Lnr: Lower non-recoverable threshold
Uc: Upper critical threshold
Lc: Lower critical threshold
Unc: Upper non-critical threshold
Lnc: Lower non-critical threshold

Table 9-8 Sensor Data Records (continued)

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/Description	Assertion Deassertion	Rearm
15	IPMC POST	Management Subsystem Health 0x28	digital Discrete 0x06	0x0 0x1	0xFF	0xFF	0x0: Performance Met 0x1: Performance Lags	Asrt	Auto
16	Boot Bank	OEM 0xD2	Sensor-specific discrete 0x6F	0x0	0xFF	0xFF	0x0: Boot Bank A	Asrt	Auto
17	Fw Progress	System Firmware Progress 0x0F	Sensor-specific discrete 0x6F	0x0 0x1 0x2	Refer *IPMI Error Logging* on page 123	Refer *IPMI Error Logging* on page 123	0x0: System Firmware Error 0x1: System Firmware Hang 0x2: System Firmware Progress	Asrt	Auto
18	OS Boot	OS Boot 0x1F	Sensor-specific discrete 0x6F	0x0 0x1 0x2 0x3 0x4 0x5 0x6	0xFF	0xFF	0x0: A: boot completed 0x1: C: boot completed 0x2: PXE boot completed 0x3: Diagnostic boot completed 0x4: CD_ROM boot completed 0x5: ROM boot completed 0x6: boot completed	Asrt	Auto
19	Boot Error	Boot Error 0x1E	Sensor-specific discrete 0x6F	0x0 0x1 0x2 0x3 0x4	0xFF	0xFF	0x0: No Bootable media	Asrt	Auto

Asrt: Assertion
Deass: Deassertion
Unr: Upper non-recoverable threshold
Lnr: Lower non-recoverable threshold
Uc: Upper critical threshold
Lc: Lower critical threshold
Unc: Upper non-critical threshold
Lnc: Lower non-critical threshold

Table 9-8 Sensor Data Records (continued)

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/Description	Assertion Deassertion	Rearm
20	Boot Initiated	System Boot Initiated 0x1D	Sensor-specific discrete 0x6F	0x0 0x1 0x2 0x3 0x4	[7:4] Active BIOS major version [3:0] Active BIOS minor version	[7:4] Active BIOS sub-minor version [3:0] Reserved	0x0: Initiated by power up 0x1: Initiated by hard reset 0x2: Initiated by warm reset 0x3: User requested PXE boot 0x4: Automatic boot to diagnostic	Asrt	Auto
21	ATCA-7360 IPMC	OEM 0xD5	Sensor-specific discrete 0x6F	0x0 0x1 0x2 0x3 0x4 0x5 0x6	-	-	0x0: Watchdog Reset 0x1: Software Reset 0x2: Power Failure 0x3: Hard Boot 0x4: Cold Boot 0x5: Warm Boot 0x6: Reserved	Asrt	Auto
22	Power Good	Entity Presence 0x25	Sensor-specific discrete 0x6F	0x0 0x1	0xFF	0xFF	0x0: Entity Present 0x1: Entity Absent	Asrt	Auto
23	POST code	OEM 0xD2	Sensor-specific discrete 0x6F	0x0 0x1 0x2 0x3 0x4 0x5 0x6 0x7	-	-	0x0: No events for this sensor. Reading according to EFI BIOS port80 status codes.	Asrt	Auto

Asrt: Assertion
Deass: Deassertion
Unr: Upper non-recoverable threshold
Lnr: Lower non-recoverable threshold
Uc: Upper critical threshold
Lc: Lower critical threshold
Unc: Upper non-critical threshold
Lnc: Lower non-critical threshold

Table 9-8 Sensor Data Records (continued)

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/Description	Assertion Deassertion	Rearm
24	Reset Source	OEM 0xD2	Sensor-specific discrete 0x6F	0x0	[7] = IPMC_RST_REQ_Payload [6] = XDP0_DBRST_CPU [5] = CPU_RST_CPU [4] RTM_PB_RST_Reset [3] = XDP1_DBRST_CPU [2] = PB_RST_Face [1] XDP0_BRD_PWROK [0] = PWR_GOOD	[7:2] = Reserved [1] = IPMC Pre-Timout [0] = IPMC Watchdog Timeout	0x0: Payload Reset detected. Cause delivered in Event Byte 2/3	Asrt	Auto
25	DDR 1 temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
26	DDR 2 temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
27	DDR 3 temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
28	DDR 4 temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
29	DDR 5 temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
30	DDR 6 temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
31	DDR 7 temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
32	DDR 8 temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto

Asrt: Assertion
Deass: Deassertion
Unr: Upper non-recoverable threshold
Lnr: Lower non-recoverable threshold
Uc: Upper critical threshold
Lc: Lower critical threshold
Unc: Upper non-critical threshold
Lnc: Lower non-critical threshold

Table 9-8 Sensor Data Records (continued)

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/Description	Assertion Deassertion	Rearm
33	DDR 9 temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
34	DDR 10 temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
35	DDR 11 temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
36	DDR 12 temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
37	IPMC temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
38	CPU Status	Processor 0x07	Sensor-specific discrete 0x6F	0x1	0xFF	0xFF	0x1: Thermal Trip	Asrt	Auto
39	CPU0 temp	Temp 0x01	Threshold 0x01		reading	threshold	uc unc	Asrt / Deass	Auto
40	CPU1 temp	Temp 0x01	Threshold 0x01		reading	threshold	uc unc	Asrt / Deass	Auto
41	-48v A Volts	Voltage 0x02	Threshold 0x01		reading	threshold	unr uc lnr lc	Asrt / Deass	Auto
42	-48v B Volts	Voltage 0x02	Threshold 0x01		reading	threshold	unr uc lnr lc	Asrt / Deass	Auto
43	-48v Amps	Current 0x03	Threshold 0x01		reading	threshold	No Thresholds		Auto
44	HoldUp Cap Volts	Voltage 0x02	Threshold 0x01		reading	threshold	unr uc lnr lc	Asrt / Deass	Auto
45	PWR Entry Temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto

Asrt: Assertion
Deass: Deassertion
Unr: Upper non-recoverable threshold
Lnr: Lower non-recoverable threshold
Uc: Upper critical threshold
Lc: Lower critical threshold
Unc: Upper non-critical threshold
Lnc: Lower non-critical threshold

Table 9-8 Sensor Data Records (continued)

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/Description	Assertion Deassertion	Rearm
46	PWR Entry Status	OEM 0xD7	Sensor-specific discrete 0x6F	0x0	Power Entry Module: [6] = VOUT_low [5] = Hotswap [4] = Holdup [2] = Alarm [1] = Enable_B [0] = Enable_A	[7:6] = Pwr Entry Module 0 = default value 1 = reserved	0x0: Pwr Entry Module Status Change detected	Asrt	Auto
47	Memory	Memory 0x0C	Sensor-specific discrete 0x6F	0x0 0x1 0x4 0x5 0x6 0x7	0xFF	[7] = CPU Socket 0/1 [6:5] = DIMM channel 0..2 [4] = DIMM number per Channel 0/1 [3:0] = DIMM number 1..12 0xF in DIMM number means unknown number	0x0: Correctable ECC 0x1: Uncorrectable ECC 0x4: Memory Device Disabled 0x5: Correctable ECC 0x6: Presence detected 0x7: Configuration error.	Asrt	Auto
48	Critical IRQ	Critical Interrupt 0x13	Sensor-specific discrete 0x6F	0x4 0x5	0xFF	0xFF	0x4: PCI PERR 0x5: PCI SERR	Asrt	Auto
49	Battery	Battery 0x29	Sensor-specific discrete 0x6F	0x1	0xFF	0xFF	0x1: Battery failed	Asrt	Auto
50	48V A Supply	Power Supply 0x08	Sensor-specific discrete 0x6F	0x0 0x1	See IPMI Spec	0xFF	0x0: Presence detected 0x1: Power Supply Failure detected	Asrt / Deass	Auto
51	48V B Supply	Power Supply 0x08	Sensor-specific discrete 0x6F	0x0 0x1	See IPMI Spec	0xFF	0x0: Presence detected 0x1: Power Supply Failure detected	Asrt / Deass	Auto

Asrt: Assertion — Unr: Upper non-recoverable threshold — Uc: Upper critical threshold — Unc: Upper non-critical threshold
Deass: Deassertion — Lnr: Lower non-recoverable threshold — Lc: Lower critical threshold — Lnc: Lower non-critical threshold

10.1 HPM.1 Firmware Upgrade

10.1.1 Overview

The primary update mechanism for the ATCA-7365 blades is the FCU tool which is delivered with the BBS package for the board. However, the ATCA-736X board family also supports upgrade of the firmware with the HPM.1 specification. Upgradable components of the board include the BIOS flash, FPGA flash, and IPMC flash. For update, it is recommended to use the Pigeon Point System modified *Ipmitool*.

10.1.2 Installing the Ipmitool

Install Procedure

1. Get the Pigeon Point System Ipmitool from the package (*Ipmitool-1.8.9-pps-7.tgz*).
2. Extract the source code.

   ```
   Prompt>tar -xzvf Ipmitool-1.8.9-pps-<version>.tgz
   ```

3. Go to the directory where you have extracted the Ipmitool.

   ```
   Prompt>cd <path>/Ipmitool-1.8.9-pps-<version>
   ```

4. Build the Ipmitool.
   ```
   Prompt>./configure && make && make install
   ```

10.1.2.1 Update Procedure

The Ipmitool HPM update requires two steps for an update:

1. Upgrade the component.
   Example: **`ipmitool hpm upgrade <file>`**
2. Activate the component.
   Example: **`ipmitool hpm activate`**

Both steps can also be integrated into one command.

```
ipmitool hpm upgrade <file> activate
```

10.1.3 Interface

The HPM.1 upgrade supports three different interfaces for upgrading the firmware. These are KCS, IPMB-0, and LAN over BASE. The LAN interface is only supported if the payload is powered on (M4). The BASE Ethernet controller also has to be powered on for this feature.

10.1.3.1 KCS Interface

The standard way to upgrade the firmware of the payload is through the KCS interface. Update through this interface is the fastest HPM.1 upgrade. The images and the Ipmi tool need to be on the payload to be upgraded.

Example:

```
Prompt>ipmitool hpm upgrade <file>
```

10.1.3.2 IPMB-0

This interface represents the backplane IPMI bus and allows remote firmware upgrade. The count of the simultaneous upgrades is limited because of the bus speed.

Example from shelf manger:

```
Prompt>ipmitool -t 0x92 hpm upgrade <file>
```

Example with RMCP+:

```
Prompt>ipmitool -I lan -H 192.168.34.8 -U Administrator -P
Administrator -t 0x92 hpm upgrade <file>
```

10.1.3.3 IPMI over LAN (BASE)

The IPMI over LAN interface uses the BASE Ethernet controller to do firmware upgrades. The interface has to be configured before the first use. Configuring this interface is described in Chapter 7, *Serial Over LAN, on page 215*.

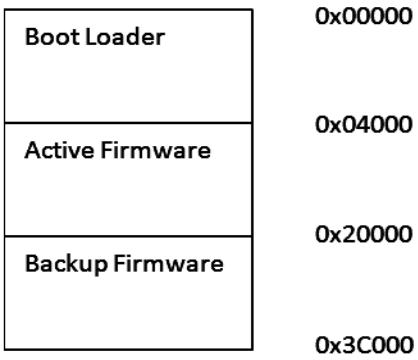
Example:

```
Prompt>Ipmitool -I lan -H 172.16.0.221 -U "" -P "" hpm upgrade
<file>
```

10.2 IPMC Upgrade

The IPMC component is fully HPM.1 compatible and contains three elements as shown on the figure below.

Figure 10-1 IPMC Component Elements



There are images for the boot loader and the firmware. There is also a combined image containing the boot loader and the firmware. The Boot loader update should only be done if it is required.

The boot loader does not perform any upgrade action. The boot loader is able to boot either of two redundant copies of the firmware in the flash depending on the current value of the special partition status byte that is stored in the internal IPMC EEPROM. The boot loader can fall back to the backup copy by booting the alternate partition. The boot loader manages two firmware partitions; the active and backup partition. It is responsible for detecting if the active firmware is invalid or has failed. If the active firmware failed or is invalid, the Boot loader will switch to the backup partition. When switching, the partitions change their roles. Switching of the partitions also take place when the firmware is upgraded and activated using the HPM.1 upgrade procedure.

The firmware image is the regular firmware and change with every update.

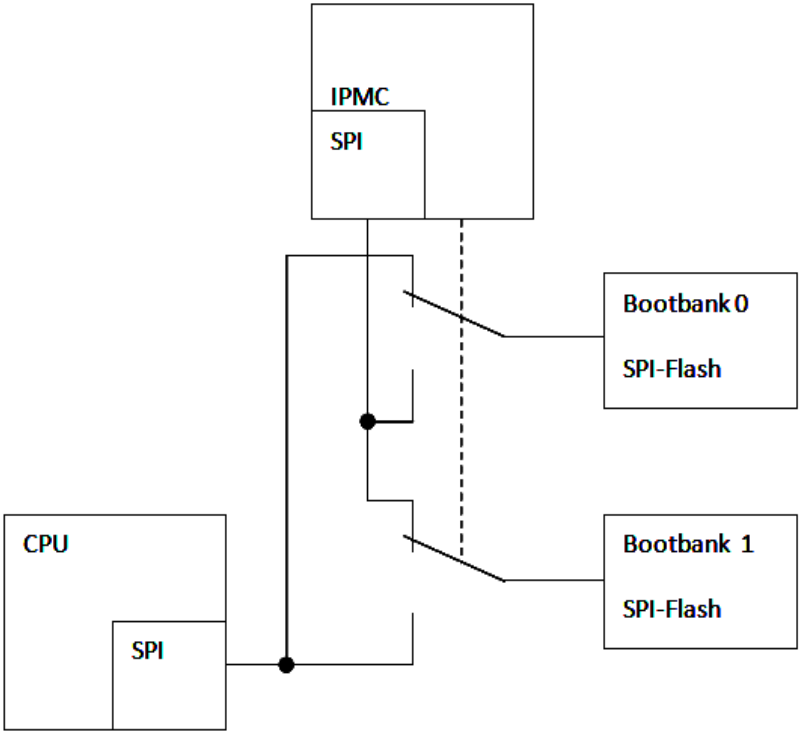
10.3 BIOS/FPGA Upgrade

Both components (BIOS and FPGA) have two independent boot banks. The switching of this boot banks is not supported by HPM commands of ATCA-736X.

Both BIOS/FPGA boot banks can be updated with HPM.1. The BIOS/FPGA upgrade is not fully HPM.1 compatible due to the fact that payload update of this device must also be possible. This leads to the fact that an automatic boot bank switching via the IPMC is not possible which is a requirement for HPM.1 to activate.

Payload always has access to the active boot bank and the IPMC always has access to the inactive boot bank. All HPM.1 commands are directed to the inactive boot bank (this includes “get component properties”). The following figure shows the connection of the SPI buses which are switched with “Set System Boot Options” -> Boot Bank (parameter 0x96). HPM activate command is not supported for the BIOS/FPGA component.

Figure 10-2 SPI Bus Connection



FPGA and BIOS upgrade may last from fifteen minutes up to two hours. The time varies with the selected programming interface. A power cycle is required after the BIOS/FPGA update.

10.4 Upgrade Package

The HPM upgrade package for this release contains the following files.

Table 10-1 HPM Upgrade Package

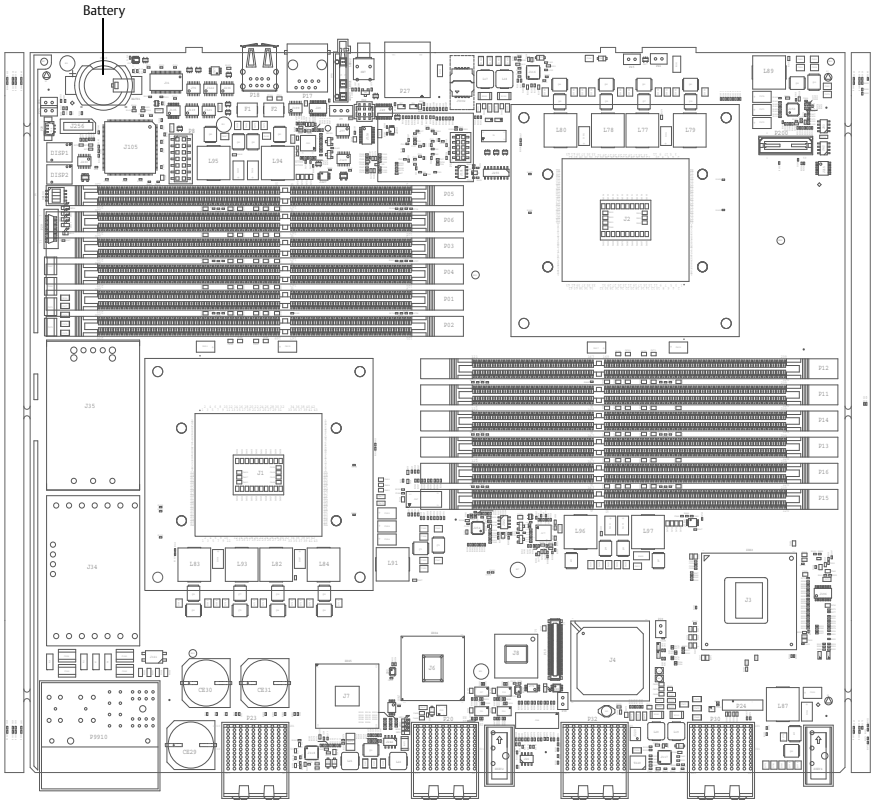
Filename	Description
atca-7360-hpm.1-all.img	HPM file contains the boot loader and firmware image
atca-7360-hpm.1-boot.img	HPM file contains only the boot loader image
atca-7360-hpm.1-ipmc.img	HPM file contains only the firmware image
9806865F07E_A736BIOS-120.bin.hpm	HPM file contains the version 1.2.0 BIOS image
atca7360_spi_13.bin.hpm	HPM file contains the version 0.13 FPGA image
Ipmitool-1.8.9-pps-7.tgz	PPS modified Ipmitool necessary for HPM upgrades on ATCA736X

A.1 Replacing the Battery

Some blade variants contain an on-board battery. Its location is shown in the following figure.

A battery-less variant based on SUPERCAP is available on demand.

Figure A-1 Location of On-board Battery



The battery provides data retention of seven years summing up all periods of actual data use. Artesyn therefore assumes that there is usually no need to replace the battery except, for example, in case of long-term spare part handling.

NOTICE

Board/System Damage
Incorrect replacement of lithium batteries can result in a hazardous explosion.
Therefore, replace the battery as described in this chapter.

Data Loss
If the battery does not provide enough power anymore, the RTC is initialized and the data in the NVRAM is lost.
Therefore, replace the battery before seven years of actual battery use have elapsed.

Data Loss
Replacing the battery always results in data loss of the devices which use the battery as power backup.
Therefore, back up affected data before replacing the battery.

Data Loss
If installing another battery type other than what is mounted at board delivery may cause data loss. This is because other battery types may be specified for other environments or may have a shorter lifespan.
Therefore, only use the same type of lithium battery as is already installed.

Replacement Procedure

To replace the battery, proceed as follows:

1. Remove battery.

NOTICE

PCB and Battery Holder Damage
Removing the battery with a screw driver may damage the PCB or the battery holder. To prevent this damage, do not use a screw driver to remove the battery from its holder.

2. Install the new battery following the "positive" and "negative" signs.

Related Documentation

B.1 Artesyn Embedded Technologies - Embedded Computing Documentation

The publications listed below are referenced in this manual. You can obtain electronic copies of Artesyn Embedded Technologies - Embedded Computing publications by contacting your local Artesyn sales office. For released products, you can also visit our Web site for the latest copies of our product documentation.

1. Go to www.artesyn.com/computing/support/product/technical-documentation.php.
2. Under FILTER OPTIONS, click the Document types drop-down list box to select the type of document you are looking for.
3. In the Search text box, type the product name and click GO.

Table B-1 Artesyn Embedded Technologies - Embedded Computing Publications

Document Title	Publication Number
RTM-ATCA-7360 Installation and Use	6806800J08
Basic Blade Services Software for the ATCA-7365 Programmer's Reference	6806800K42
ATCA-7365-CE Quick Start Guide	6806800L74
ATCA-7365-CE Safety Notes Summary	6806800L75

B.2 Manufacturers' Documents

For additional information, refer to the following table for manufacturers' data sheets or user's manuals. As an additional help, a source for the listed document is provided. Please note that, while these sources have been verified, the information is subject to change without notice.

Table B-2 Manufacturer's Documents

Company	Document Title
Intel	6300ESB I/O Controller Datasheet 82546EB/GB Gigabit Ethernet Controller Documentation 6700PXH 64-bit PCI-to-PCI bridge Datasheet E7520 Memory Controller Datasheet IPMI V1.5 Specifications Intel® Xeon™ Processor Technical Documents
LSI Logic	LSIFC929XL Dual-Channel PCI-X to Fibre Channel Controller Technical Documents
SMSC	LPC47S422 Enhanced Super I/O Controller Datasheets and Application Notes

B.3 Related Specifications

For additional information, refer to the following table for related specifications. As an additional help, a source for the listed document is provided. Please note that, while these sources have been verified, the information is subject to change without notice.

Table B-3 Related Specifications

Organization	Document Title
PCI-SIG	PCI Local Bus Specification Revision 2.2 PCI-X Addendum to the PCI Local Bus Specification 1.0
PICMG	PICMG 3.0 Revision 2.0 Advanced TCA Base Specification PICMG 3.1 Revision 1.0 Specification Ethernet/Fiber Channel for AdvancedTCA Systems